LOW MASS MEMS/NEMS SWITCH FOR A SUBSTITUTE OF CMOS TRANSISTOR USING SINGLE-WALLED CARBON NANOTUBE THIN FILM

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Dedication

I dedicate this dissertation to my wife and parents.

Abstract

Power dissipation is a key factor for mobile devices and other low power applications. Complementary metal oxide semiconductor (CMOS) is the dominant integrated circuit (IC) technology responsible for a large part of this power dissipation. As the minimum feature size of CMOS devices enters into the sub 50 nanometer (nm) regime, power dissipation becomes much worse due to intrinsic physical limits. Many approaches have been studied to reduce power dissipation of deeply scaled CMOS ICs. One possible candidate is the electrostatic electromechanical switch, which could be fabricated with conventional CMOS processing techniques. They have critical advantages compared to CMOS devices such as almost zero standby leakage in the off-state due to the absence of a pn junction and a gate oxide, as well as excellent drive current in the on-state due to a metallic channel.

Despite their excellent standby power dissipation, the electrostatic MEMS/NEMS switches have not been considered as a viable replacement for CMOS devices due to their large mechanical delay. Moreover, previous literature reveals that their pull-in voltage and switching speed are strongly proportional to each other. This reduces their potential advantage. However, in this work, we theoretically and experimentally demonstrated that the use of single-walled carbon nanotube (SWNT) with very low mass density and strong mechanical properties could provide a route to move off of the conventional trend with respect to the pull-in voltage / switching speed tradeoff observed in the literature.

We fabricated 2-terminal fixed- beam switches with aligned composite SWNT thin films. In this work, layer-by-layer (LbL) self-assembly and dielectrophoresis were

selected for aligned-composite SWNT thin film deposition. The dense membranes were successfully patterned to form submicron beams by e-beam lithography and oxygen plasma etching. Fixed-fixed beam switches using these membranes successfully operated with approximately 600 psec switching delay and as low as a 3 V dc pull-in. From this we confirmed that the SWNT-based thin films have the potential to make fast MEMS switches with a low operation voltage due to its low mass density and high stiffness. However, the copolymer caused a serious reliability issue and a copolymer-free SWNT film deposition method was developed by replacing positive copolymer with a dispersion of positively functionalized SWNTs.

The electrical and physical properties of pure single-walled carbon nanotube thin films deposited through a copolymer-free LbL self-assembly process are then discussed. The film thickness was proportional to the number of dipping cycles. The film resistivity was estimated as $2.19 \times 10^{-3} \Omega \cdot cm$ after thermal treatments were performed. The estimated specific contact resistance to gold electrodes was $6.33 \times 10^{-9} \Omega \cdot m^2$ from contact chain measurements. The fabricated 3-terminal MEMS switches using these films functioned as a beam for multiple switching cycles with a 4.5V pull-in voltage, which was operated like a 2-input NAND gate. The SWNT-based thin film switch is promising for a variety of applications to high-end nanoelectronics and high- performance MEMS/NEMS.

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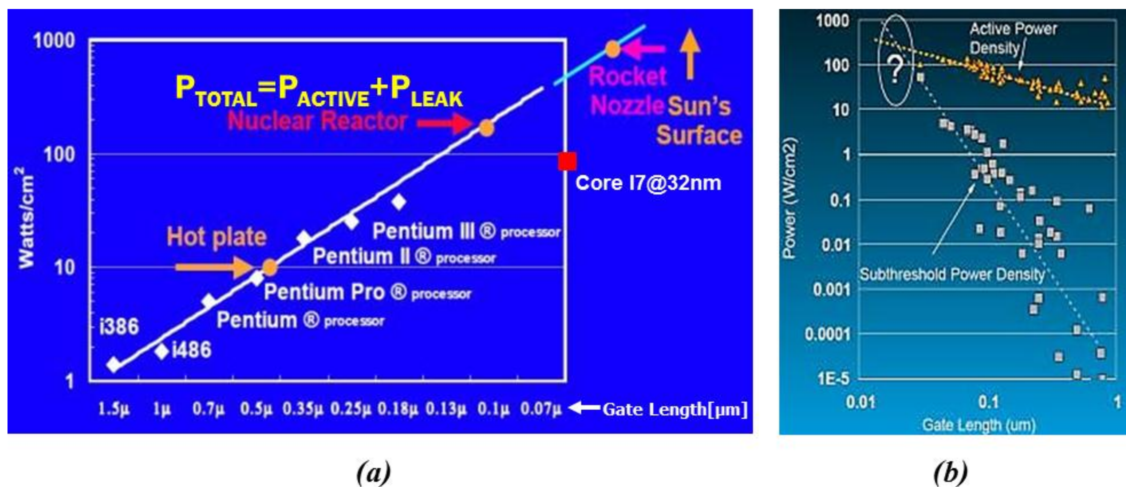
CHAPTER 1: INTRODUCTION

1.1. Power Dissipation Problem in scaled CMOS Technology

Power dissipation is a key factor for mobile devices and other low power applications. Complementary metal oxide semiconductor (CMOS) is the dominant integrated circuit (IC) technology responsible for a large part of this power dissipation. CMOS ICs have two major components of power dissipation, standby power dissipation and active power dissipation. The former is due to leakage currents such as subthreshold leakage, junction leakage and gate leakage. The latter is due to switching operation such as charging and discharging load capacitances, and the short circuit that occurs briefly during typical switching transients when all CMOS devices are turned on. As the minimum feature size of CMOS devices enters into the sub 50 nanometer (nm) regime,



(a) *(b)*

Figure 1.1. (a) A trend of power dissipation density as scaled down of Intel CPUs; Reproduced from [3], and (b).Active power dissipation density versus subthreshold power dissipation density; Reproduced from [4].

the power dissipation becomes much worse due to the intrinsic physical limits such as short channel effects [1-2]. For example, a new Intel CPU chip with 32 nm technology consumes almost 100 watts per square centimeter, which is close to that of a nuclear reactor [3] as shown in Figure 1.1(a). Furthermore, at the 25 nm technology regime, Nowak *et al* forecasted the power consumption due to standby leakage might be comparable to the active power consumption [4], as shown in Figure 1.1(b). This exponentially increasing standby leakage current of CMOS devices as they are scaled down, as a result, deteriorates the battery life time and requires more stringent cooling systems to suppress the excessive heat generation [3-4]. Therefore, there is a strong need to seek a way to mitigate this power dissipation issue in terms of both new device technology development and circuit level techniques. Our work originates from the former approach.

1.2. Efforts to Reduce CMOS Power Dissipation

In order to mitigate the power dissipation issue of CMOS devices, extensive efforts have been performed such as optimization of conventional devices and development of new concept devices as well as the circuit techniques. In this section, each approach is discussed.

1.2.1. Device Level

In the device perspective, there are two approaches to resolve the power dissipation

issue of CMOS devices such as optimizing the conventional device structures and materials or developing a new concept device using nanotechnology. The former approaches are, for example, high-k/metal gate [12, 13], strained-silicon [14], 3-dimensional field effect transistors (FET) such as multi-gate Fin-FET [15] and recessed channel FET [16]. These approaches were already commercialized or will be in the very near future. However, they have still intrinsic physical limitations in the power dissipation because they are still based on conventional CMOS device physics. The latter approaches, new concept materials and devices, have been reported such as tunnel field effect transistors (FET) [17], single electron transistor [18], carbon nanotube/graphene FET [19], and so on. Until now, however, it is not clear which device could substitute the conventional CMOS devices because a new concept device should meet all of the following requirements to be successful as a substitute of CMOS:

(1) It can reduce the standby power dissipation without degrading the drive current.

(2) Its process is controllable as well as compatible to conventional CMOS process.

(3) It can be scalable into the nanometer regime.

1.2.2. Circuit Level

There are two possible ways to mitigate the power dissipation. One is to improve circuit performance without further scaling down to single nanometers region and the other is to reduce power dissipation itself for lower power density. To improve circuit performance, both parallelism and pipelining have been used [5]. If the total power dissipation were independent of scaling, the power density of a chip would increase,

which results in increasing the temperature of chip. At high temperature, the characteristics of the MOSFET degrade. Typical effects include increased leakage and decreased drive current [6]. Therefore, a more aggressive cooling systems have been used to suppress the excessive heat generation. Furthermore, the power dissipation itself should be reduced. The power dissipation in CMOS devices consists of active power dissipation and standby power dissipation as introduced. For lower active power dissipation, lower operating voltage, smaller node capacitance and slower frequency would be preferred [3-4, 6]. For lower standby power dissipation, body-biasing [7], power-gating with sleep transistors using a dual threshold voltage [8] and clock gating [9] have been considered. However, these approaches require the user to sacrifice the circuit performance or to add overhead to make up the loss of performance or significant circuit modification [10]. Some of these approaches would not be useful if the gate oxide leakage and band-to-band tunneling leakages are comparable to subthreshold leakage [11]

1.2.3. Summary

Many approaches have been studied to reduce power dissipation of deeply scaled CMOS ICs, using both device and circuit perspectives. However, these approaches generally unavoidable drawbacks and require sacrifices in the performance and cost to implement. Therefore, there is a strong need to find an emerging technology, which has nearly zero leakage current, but has high drive current, that also can utilize CMOS fabrication and design concepts, and can be integrated with CMOS technology without additional overhead.

1.3. Electrostatic MEMS/NEMS Switches

Microelectromechanical systems (MEMS)/nanoelectromechanical systems (NEMS) are the integrated micro/nanosystems comprising electronic and mechanical components, which are fabricated with conventional CMOS processing techniques and range from tens of nanometer to millimeters in sizes. Based on their applications, the MEMS/NEMS could be classified into four categories: sensors, actuators, switches, and resonators. Electrostatic MEMS/NEMS switches are operated by electrostatic force. They have critical advantages compared to CMOS devices such as almost zero standby leakage at off-state due to the absene of pn junction or a gate oxide and excellent drive current in the on-state due to a metallic channel. In this section, their operation principles, merit and drawbacks are discussed in detail.

1.3.1. Principle of Operation

Typically, the electrostatic MEMS/NEMS switches consist of a movable electrode or suspended beam/plate and multiple fixed electrodes. And they are operated by the application of an electrostatic force between a movable/suspended beam and a fixed electrode (or multiple electrodes) due to the imposition of a potential difference. In addition to the electrostatic force, van der Waals (vdW) force and short range forces may attract the movable beam down to the fixed electrode(s) or another movable beam [21].

When the electrostatic force and other forces overcome the elastic force of the movable beam, the movable beam abruptly contacts down to the fixed electrode [21]. The required electric voltage for this transition from OFF-state to ON-state is known as “Pull-

in voltage". If short range forces are small compared to the mechanical restoring force, the device is turned off when the actuating voltage is removed. Therefore, MEMS/NEMS switches could provide almost off-leakage free and abrupt switching characteristics, which would be preferable for low power applications. The electrostatic MEMS/NEMS switches have several typical designs depending on the structures and actuating directions including cantilevers and fixed-fixed beams (Figure 1.2). Both cantilever and fixed-fixed beam types have unique advantages and disadvantages. Generally, the cantilever type switches has lower operation voltage than fixed-fixed type, due to their lower spring constant [20].

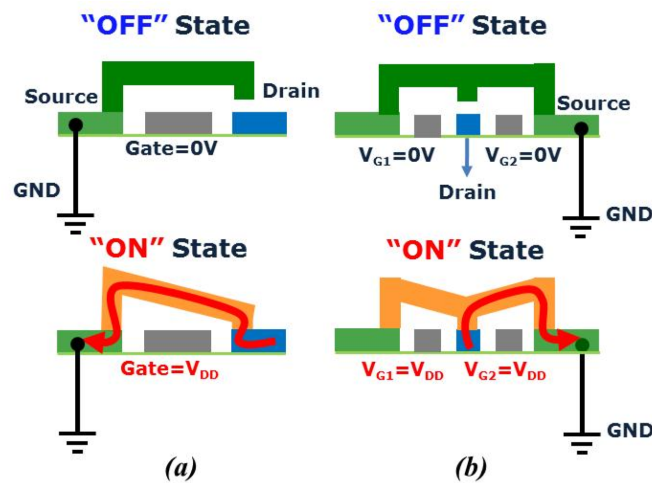


Figure 1.2. 3-terminal MEMS/NEMS switches: (a) Cantilever type and (b). Fixed-Fixed beam type

However, when the cantilever layer has large residual stress, it may easily curled or collapse. The fixed-fixed beam type switches have two anchors at the both ends so it is

structurally more rigid. This results in a higher spring constant than cantilevers with same material and dimensions.

Conceptually, 3-terminal MEMS switches have almost zero standby leakage and could work as either n-type or p-type device depending on bias conditions. Figure 1.3 shows an inverter configuration with two 3-terminal MEMS switches. In this manner, we could implement most kinds of digital logic circuits instead of CMOS devices.

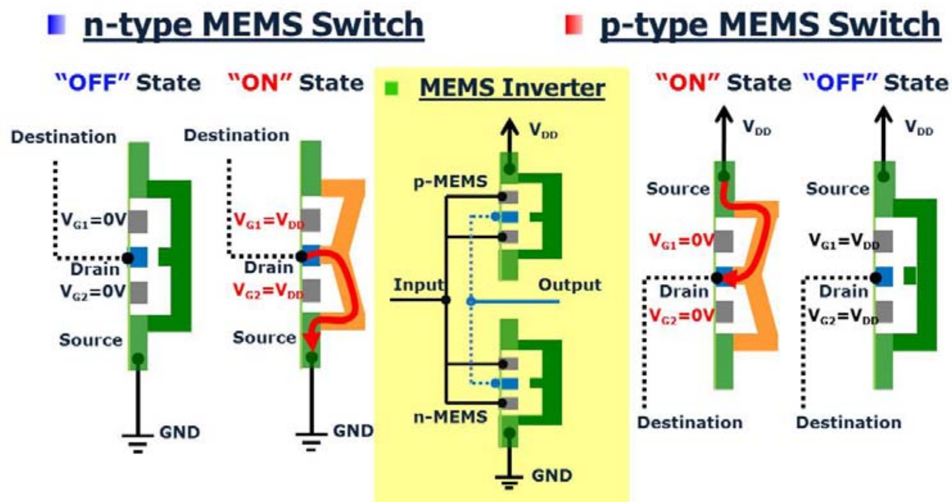


Figure 1.3: An example of the MEMS inverter configuration with two 3-terminal devices.

1.3.2. Key Design Constraints

To be a competitive alternative to solid state devices, MEMS switches must be capable of high speed operation with low actuation voltages, in other words, pull-in voltage, as well as possess comparable reliability to CMOS devices.

1.3.2.1. Pull-In Voltage

In the MEMS/NEMS devices, this is conceptually analogous to the threshold voltage in the CMOS devices, which means a specific voltage that switch is "turned-on" so that an electrical current can flow through it. The pull-in voltage is dependent on the stiffness of suspended beam material and device dimensions [22] as below. This will be discussed in more detail in the Chapter 2.

$$V_{pull-in} \propto \frac{t}{L^2}\sqrt{E}\sqrt{Ltd_0^3} \tag{1.1}$$

,where t, L, E, d_0^3 are the thickness, length, and Young's modulus of suspended beam and the air-gap between suspended beam and bottom fixed electrode, respectively. Therefore, in the device design stage, we have to carefully select the material and device dimensions to get the predetermined pull-in voltage target.

1.3.2.2. Switching Speed

In considering the both ends fixed beam with concentrated loading at its center, its switching speed (*s*) is directly proportional to the natural frequency of vibration (*f*) of the spring-mass system [23], which is dependent on the stiffness, mass density and dimensions of the beam as below [22].

$$s \propto f \propto \frac{t}{L^2}\sqrt{E}\sqrt{\frac{1}{\rho}} \tag{1.2}$$

Where ρ is the mass density of the beam.

1.3.2.3. Reliability

In switching, the suspended beam is deflected by electrostatic force. This process generates a stress on the beam. The maximum tensile stress (σ) is related to device dimensions and stiffness of the suspended beam and should be smaller than tensile strength [24, 25] for reliable operations as below.

$$\sigma_{max} = 1.5E\frac{d_0 t}{L^2} \leq Yield\ strength \quad (1.3)$$

However, inherently, the MEMS/NEMS switches are subjected to repeated stress cycles, which may cause an early failure at a stress significantly lower than the yield strength [22]. The fatigue-induced damage of MEMS/NEMS structures is currently a topic of active research [26]. The fatigue life of a device is typically evaluated experimentally and

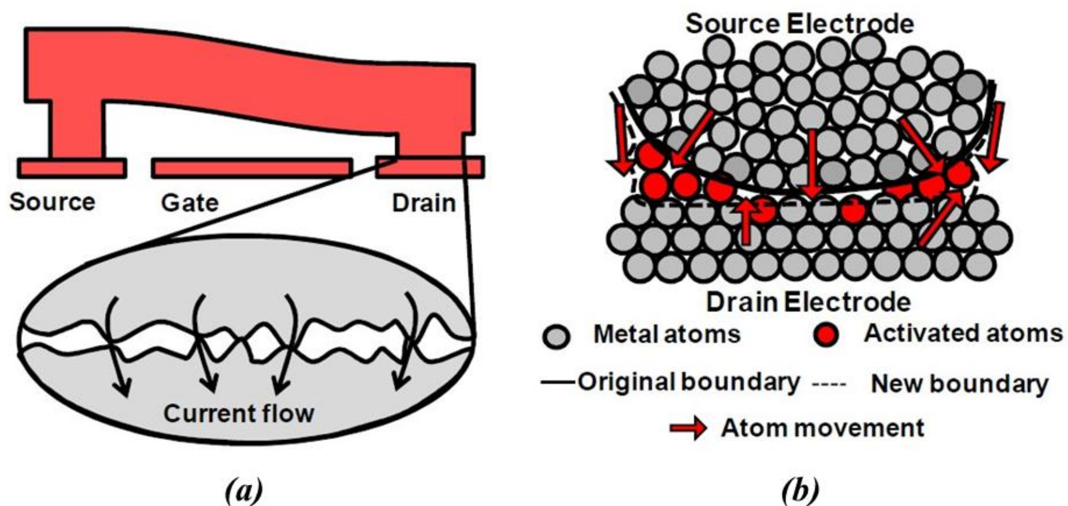


Figure 1.4: (a) The on-state conductance of a MEM switch is limited by asperities on the contacting metallic surfaces, (b) Thermally activated metal-atoms diffuse across the contacting surfaces and eventually fill the voids in between ; Reproduced from [27].

anecdotal evidence suggests that the resistance to fatigue increases with decreasing length scale [22].

Another issue to consider is the contact reliability between a suspended beam and the bottom electrode. Cyclic and repeated switching operation may cause a substantial Joule heating at the contacting asperities which eventually leads to welding-induced failure as shown in Figure 1.4 [27]. Kam *et al* demonstrated the endurance can be improved by increasing on-state resistance of MEMS/NEMS switches and by reducing the supply voltage and load capacitance through an atomic diffusion based model for predicting the endurance of a MEMS switch, which was validated experimentally [27].

1.3.3. Literature Review

In the literature, many studies have reported 2-terminal [28-32], 3-terminal [33-42], and 4-terminal [42-47] electrostatic MEMS/NEMS switches. A typical 2-terminal electrostatic MEMS/NEMS switch has a movable/suspended beam and a fixed electrode. Kim *et al* [29] reported two types of two terminal NEMS switches, the NEMS cantilever switch (NCLS) and the NEMS clamp switch (NCS) which is a fixed-fixed beam switch. These were fabricated using a conventional CMOS fabrication process as shown in Figure 1.5. Polycrystalline silicon (poly) was used as a sacrificial layer to form an ultra-thin uniform air gap on top of the shallow trench isolation (STI). TiN was used for the beam due to its high stiffness and low electrical resistivity to get reliable operation of NEMS switches [29]. To release switches, an exposed poly-Si mask and sacrificial layer were removed by a wet etchant that had a very high etch selectivity to both the TiN beam

and the field oxide [29]. These switches had 10~15V of pull-in voltages and about 5V of hysteresis between pull-in and pull-out [29]. Although the switching time was not reported, they reported that the fixed-fixed type switch demonstrated a good pulse response to an AC signal, under the AC bias sweep condition (f=5 Hz, t=several tens of seconds) [29]. A variety of materials have been reported as a suspended beam for 2-terminal switches such as carbon nanotube (CNT) thin films [28], tungsten [30], AlSi [31], and a single CNT bundle [32]. 2-terminal MEMS/NEMS switches with sufficienct hysteresis could be used as a memory device [29] and a suspended gate for a nanoelectromechanical FET (NEMFET) [31].

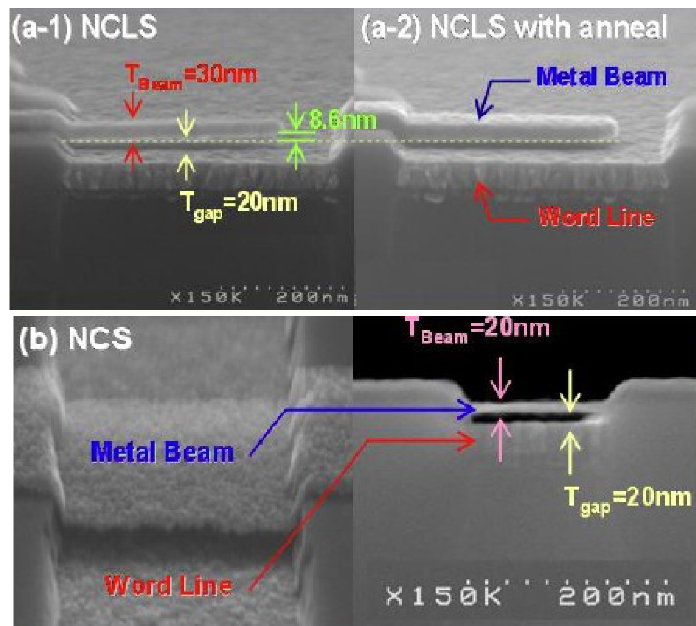


Figure 1.5: An example of the MEMS inverter configuration with 2-terminal devices using TiN as a suspended metal beam, (a) Cantilever type switch (NCLS), (b) Fixed-Fixed type switch (NCS); Reproduced from [29].

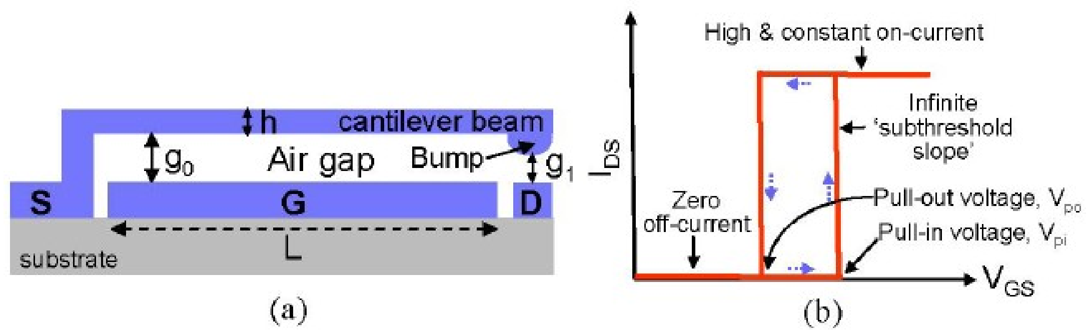
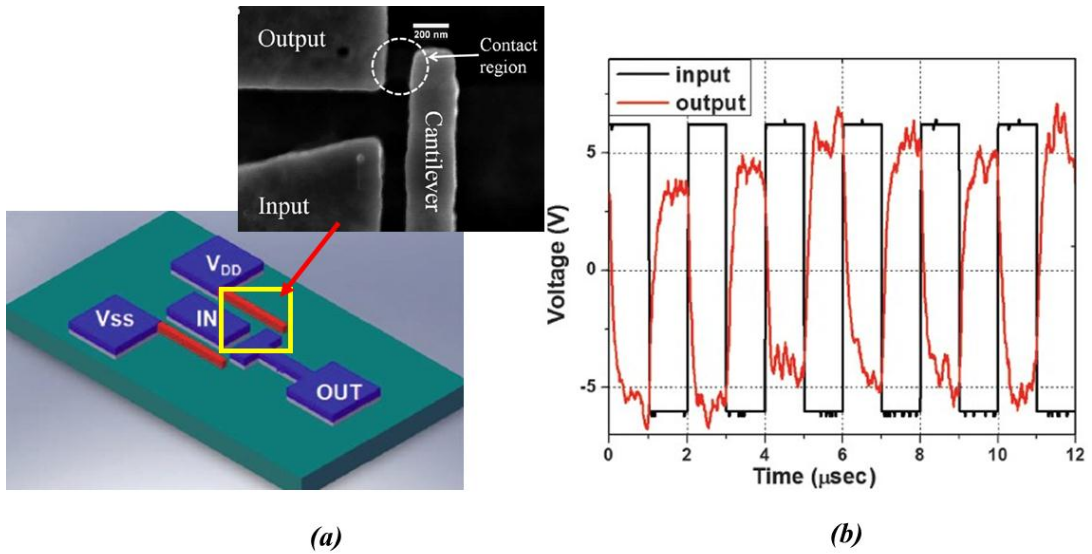


Figure 1.6: An example of the MEMS inverter configuration with 3-terminal devices, (a) a cross-sectional schematic, (b) a typical I-V curve showing pull-in and pull-out voltage; Reproduced from [34].

Akarvardar *et al* [34] estimated the merits and de-merits of the 3-terminal NEMS switch (Figure 1.6) logic gates compared to CMOS logic gates in terms of the scaling, density, speed and energy consumption for various materials. At CMOS-compatible supply voltages, the switching speed of the conventional NEMS switches hardly achieves GHz range due to the large mechanical delay associated with the beam movement. This delay makes typical NEMS devices slower than current CMOS devices [34]. However, the electrostatic NEMS switches are unchallenged for the applications where the reduction of the static power is the main concern and possess excellent dynamic power advantages [34].

MEMS/NEMS logic gates may also be advantageous for operating at high temperatures compared to CMOS devices, which require expensive heat-sinking and thermal-management [33]. Lee et al [33] implemented a 3-terminal cantilever based MEMS inverter with silicon carbide as a suspended beam for working at 500˚C as shown



(a) *(b)*

Figure 1.7: An example of a MEMS inverter configuration with 3-terminal devices, (a) a schematic of an inverter with silicon carbide cantilevers, (b) an input-output voltage waveform of the inverter at 500˚C; Reproduced from [33].

in Figure 1.7. The two laterally actuated cantilevers of the inverter are connected to positive- (V_{DD}) and negative-voltage (V_{SS}) terminals, respectively. When applying a positive input (logic high), the electrostatic force between the input and the cantilever connected to V_{SS} overcomes the restoring force of the beam, and the cantilever moves laterally to contact the output, providing a logic low. A logic high can be obtained by supplying a negative input to actuate the beam connected to V_{DD}. Switches have been verified to work at 500°C in a nitrogen environment to prevent surface oxidation with V_{DD}=6Vand V_{SS} = –6V, at an operating speed of 500 kHz. [33].

However, there is no way to modulate the pull-in voltage electrically in electrostatic MEMS/NEMS switches. It depends on the physical properties of the beam material and

the device dimensions such as air gap, beam length and thickness. Nathaniel *et al* [45] demonstrated 4-terminal MEMS switches with a CMOS-compatible process as shown in Figure 1.8.

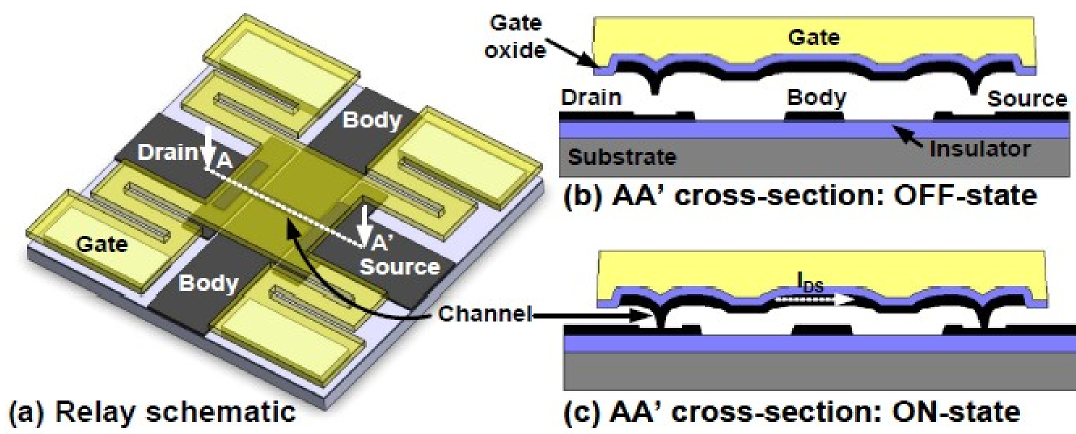


Figure 1.8: Schematic illustrations of the four-terminal relay structure. (a) Isometric view. (b) Cross sectional view along the channel (AA') in the off-state. (c) Cross-sectional view in the on-state. The gate is actuated downward by applying a gate-to-body voltage (V_{GB}); Reproduced from [45].

The 4-terminal design provides a means for electrically adjusting the pull-in voltage (via a body terminal). By forcing a bias at the body electrode, the pull-in voltage may be modulated electrically in a device as shown in Figure 1.9. As the body bias decreases from 4V to -8.5V, the pull-in voltage also decreases from 8V to less than 2V.

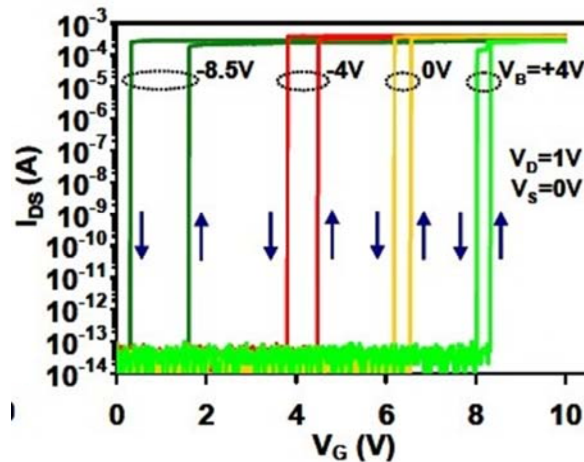


Figure 1.9: Measured I_{DS}-V_G characteristics of a single 4-terminal MEMS switch, with V_S=0V depending on body voltage; Reproduced from [45].

Since electrostatic MEMS/NEMS switches can be made complementary with the appropriate choice of body voltage, many of the logic styles used in CMOS can be directly extended to relay-based designs [47]. However, the electrical characteristics and behavior of MEMS/NEMS switches are significantly different than that of CMOS transistors. The delay of a single CMOS transistor is largely set by the time it takes to charge or discharge the output capacitance. In contrast, for a MEMS/NEMS switch, the delay is dominated by the time it takes to mechanically displace the beam [45].

1.3.4. Issues of Traditional Electrostatic Mechanical Switches

Despite excellent standby leakage at off-state and low channel resistance at on-state, the electrostatic MEMS/NEMS switches have an inherent problem in their switching speed, mostly due to mechanical dely. From the literature, the pull-in voltage and switching speed of conventional electrostatic MEMS/NEMS switches are largely

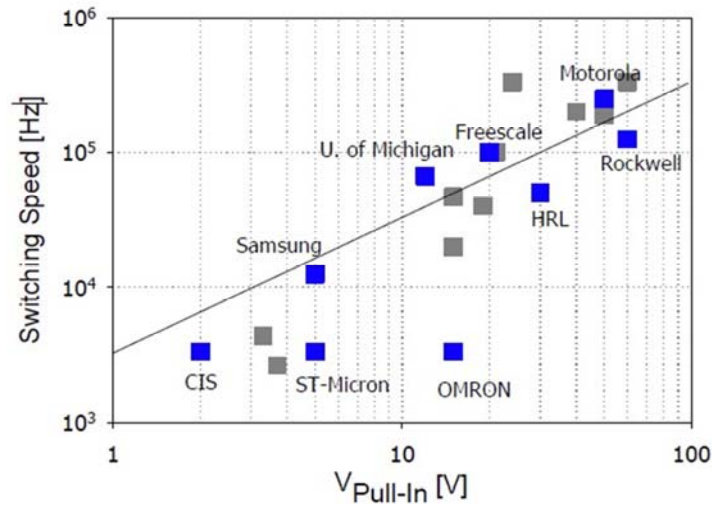


Figure 1.10: Switching speed versus actuation voltage from literatures. The line indicates a unity slope. Reproduced from [49].

proportional to each other as shown in Figure 1.10 [49]. This relationship can be understood from the equations 1.1 and 1.2 which show that the pull-in voltage and switching speed have a common term, $\left(\frac{t}{L^2}\sqrt{E}\right)$. This means that it is difficult for a high switching speed device to also have a low operating voltage. This would be a major drawback for a high-speed, high-density, low-power logic application. Moreover, many studies have used chemical vapor deposition for suspended beam material deposition. The high temperatures required for this process would degrade pre-existing CMOS devices if the MEMS/NEMS switches are made after CMOS fabrication. This lack of compatibility prevents a gradual development of a technology since one could not use it as a CMOS enhancement.

1.4. Our Approach to Overcome These Problems

From the literature, the large mechanical delay may be a drawback to implement MEMS/NEMS basic logic circuits equivalent to CMOS. Most efforts to improve switching speed would result in higher pull-in voltage. However, Equations 1.1 and 1.2 suggest two independent parameters: the air-gap and the beam mass density. Reducing both could be a route to low power and high switching speed which would move off of the trend shown in Figure 1.10.

The minimum air-gap is determined by the sacrificial layer thickness and the etch process limit. The smallest reported air-gap is 7nm [54]. The major concern with very small gaps is avoiding stiction, the collapse of the device upon release. The material selection for a suspended beam needs to be more cautious because it would determine the

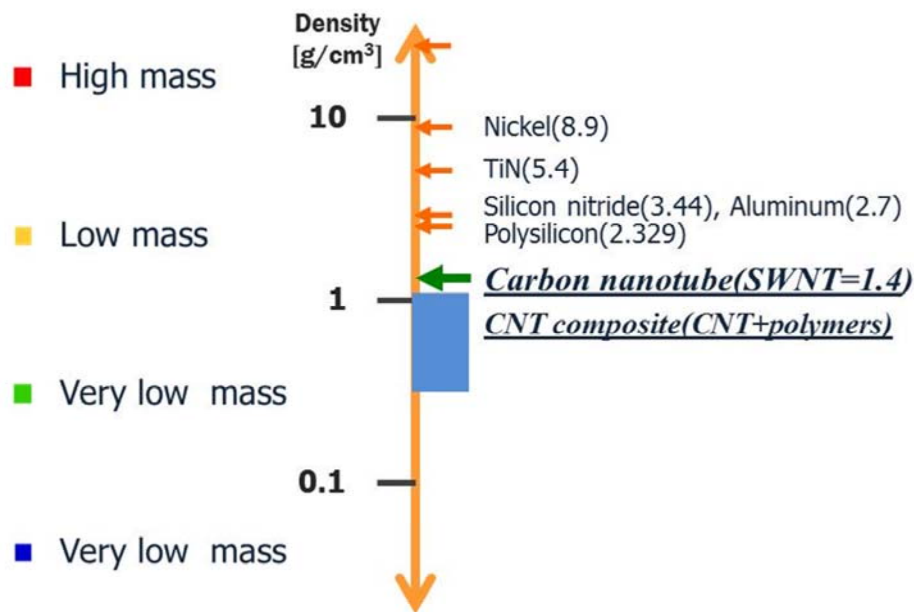


Figure 1.11: Mass density of beam materials from literatures.

overall characteristics of the fabricated MEMS/NEMS switches. Figure 1.11 shows the mass density of suspended beam materials from reported literature such as polysilicon [50], silicon nitride [51], aluminum [52], TiN [29], Nickel [53], gold [54]. As mentioned, a new material with a lower mass density than conventional materials and a higher yield strength would help achieve the goal of low-power high-speed reliable NEMS. A high Young's modulus is also helpful since it allows one to achieve higher speed at a given lithography capability.

Carbon nanotubes (CNT) can meet all of these requirements since they have a low mass density (~1.4g/cm^3) and excellent mechanical properties (Young's modulus about 1 TPa, Yield strength about 2 TPa), as will be discussed in the Section 1.5. CNT-polymer composite materials could provide the opportunity for even lower mass density. Extensive studies have been performed to implement CNT based MEMS/NEMS switches [28, 32, 39, 40]. Kaul *et al* [32] demonstrated laterally grown single-walled carbon

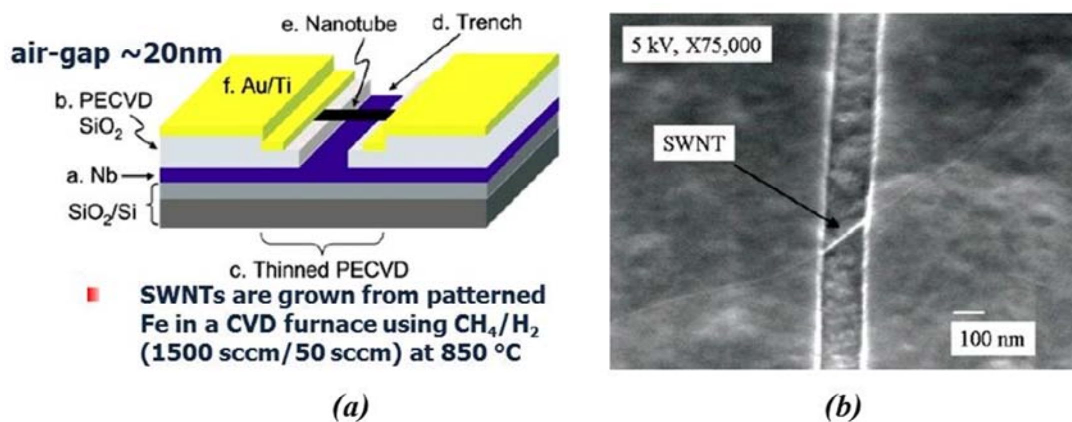


Figure 1.12: (a) A schematic of 2-terminal NEMS switch based on single-walled carbon nanotube by chemical vapor deposition process, (b) a scanning electron microscopy image of fabricate device; Reproduced from [32].

nanotube (SWNT) based 2-terminal NEMS switch using chemical vapor deposition with pre-patterned Fe catalyst as shown in Figure 1.12. They reported that fabricated 2-terminal switches had 1.5~2.0V of pull-in voltage and 2.8ns of switching delay.

Jang *et al* [39] demonstrated 2-terminal and 3-terminal NEMS switches using vertically grown multi-walled carbon nanotube (MWNT) by chemical vapor deposition with patterned nickel catalyst as shown in Figure 1.13. Measured pull-in voltages ranged from 22 to 27V. The switching speed was not reported.

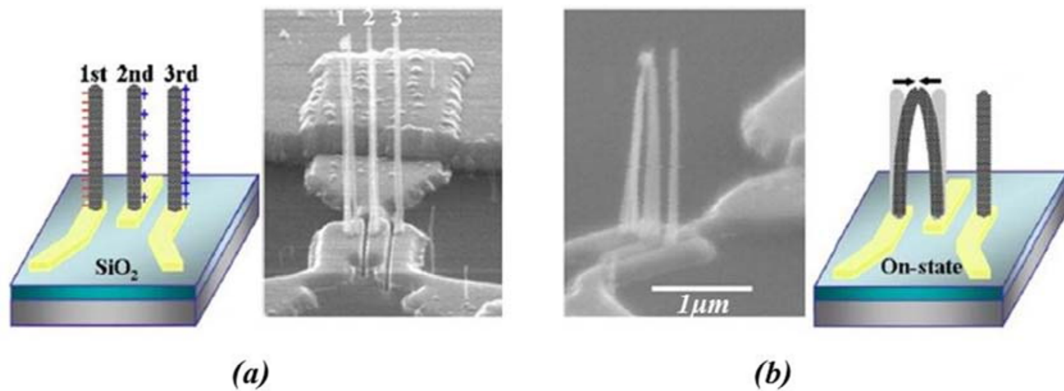


Figure 1.13: A schematic of 3-terminal NEMS switch based on multi-walled carbon nanotube by chemical vapor deposition process, (a) a schematic and scanning electron microscopy image at off-state, and (b) at on-state; Reproduced from [39].

Most studies have used a single bundle as a suspended beam and have fabricated the bundle using chemical vapor deposition at high temperature (>600˚C). However, the current carrying capacity of individual CNTs or even small bundles is too small to meet the requirements of MEMS and NEMS [56-57]. Also the high temperature process has a limitation in some applications as mentioned in the previous section. To overcome these limitations, we would need a CNT-based thin film, which should be deposited at low

temperature. In addition, the deposition process should be controllable and extendable to a whole wafer. In this work, the layer-by-layer self-assembly process was used. This will be discussed in the Chapters 3, 4, and 5 in more detail.

1.5. Carbon Nanotubes

Since Iijima in 1991 reported the CNT for the first time [58], it has been extensively studied and used as a physical/electrical backbone material for a variety of applications due to their unique properties [59]. A CNT can be described as a seamlessly rolled-up sheet of graphene, resulting in an open tubular structure composed of carbon atoms arranged in a hexagonal network [59]. Single-walled CNTs (SWNT) and multi-walled CNTs (MWNT) are shown in Figure 1.14. For SWNTs, there are three different ways in which a graphene sheet can be rolled up onto itself: armchair, zig-zag, and, more generally, chiral SWNT as shown in Figure 1.15.

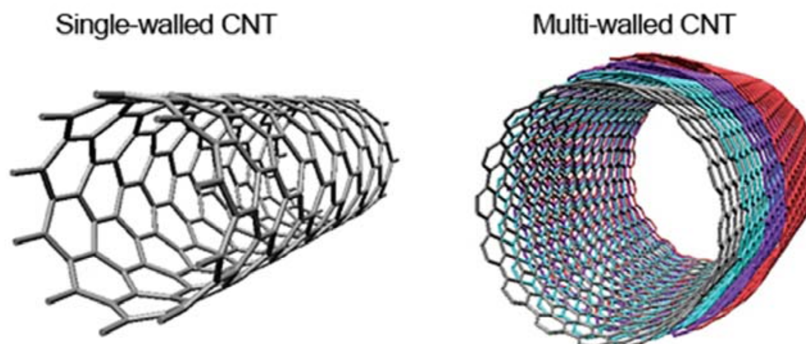


Figure 1.14: A schematic of SWNT (left) and MWNT (right); Reproduced from http://science.uwaterloo.ca/~foldvari/research_program/index.html.

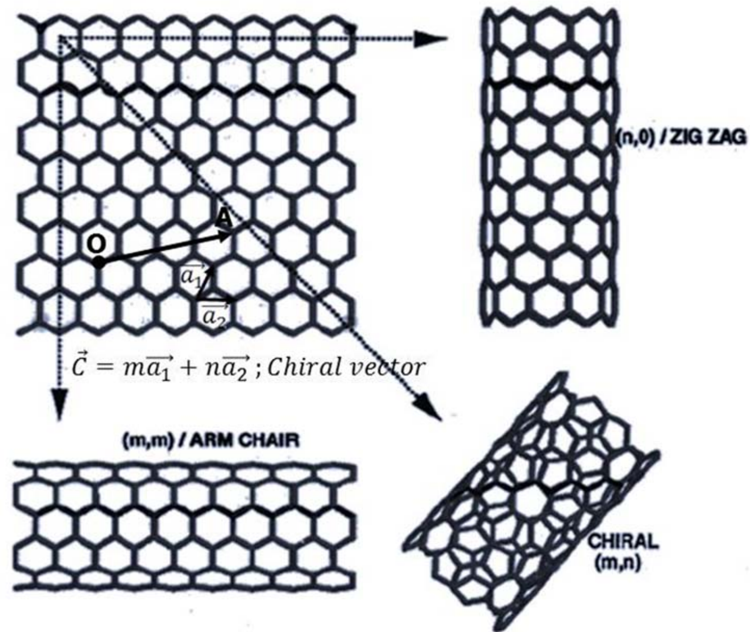


Figure 1.15: A schematic of 3-different types of SWNT depending on how a graphene sheet is rolled up onto itself: armchair, zig-zag and the more general chiral; Reproduced from [60].

The armchair tubes are obtained when the carbon-carbon bounds are perpendicular to the cylinder axis, which looks like an "armchair" at the cross-section. The zig-zag tubes are obtained when the carbon-carbon bounds are parallel to the tube axis. Chiral tubes are obtained when the hexagons of the original graphene sheet are wound around tube axis in a helical way along the length of the tube. In any case, the structure of the nanotubes easily can be described by so-called chiral vector $\vec{C}$. It is composed of a two-dimensional pair of integer numbers (m, n) corresponding to the numbers of the hexagonal unit cell vectors $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$, respectively, needed to roll-up the graphene sheet onto itself from one point to another. Armchair type SWNTs can be expressed as (n,n) and zig-zag type SWNTs as (n,0). Typically, SWNTs have diameters of about 1 nm and

lengths up to several micrometers, according to experimental observations [59].

Three main methods have been used to synthesize carbon nanotubes: Arc-discharge, laser ablation, and chemical vapor deposition (CVD) [59]. The first two techniques use solid-state carbon precursors and require very high temperatures (thousands of degrees Celsius) [61]. These methods are well established in producing high-quality and nearly perfect nanotube structures. However, they also produce large amounts of byproducts associated with them. CVD technique use hydrocarbon gases and metal catalyst particles as “seeds” for nanotube growth. Growth takes place at relatively lower temperatures (500-1000 °C) [61].

An ideal CNT is composed of only carbons in an open structure and so it has very low mass density (~1.4 g/cm^3). Due to strong carbon-carbon bounds, it has a Young’s modulus larger than 1TPa and its tensile strength ranges from 11 GPa to 150 GPa [62]. Experimentally it has been found that SWNTs show ballistic transport even at room temperature, have current densities as high as 10^{10} A/cm^2 (copper and aluminum show values between 10^7 and 10^{10} A/cm^2), and behave as excellent electron emitters with low turn-on fields of 1.5–5 V/μm at 1 mA/cm^2 and low energy spread of 0.25 eV [59].

Due to their excellent properties, CNTs have a great potential for applications in various technological fields, which are ranged from nanoelectronics, flexible plastic electronics, functional composite, energy, nanobio, and nanocatalyst dispersions [59, 61].

1.6. Thesis Overview

Despite excellent standby leakage power dissipation, the MEMS/NEMS switches have not been a successful replacement of CMOS devices due to their large mechanical delay. To resolve this problem, it is necessary to develop a new suspended beam material with low mass density and high stiffness as well as to understand the operation principle of MEMS/NEMS switches. Chapter 2 reviews the operation principle and key parameters of MEMS/NEMS switches through theoretical approaches. Chapter 3 reviews the CNT based thin film deposition techniques from literature. Chapter 4 demonstrates the fabrication and characteristics of 2-terminal NEMS switches using aligned composite SWNT thin films and presents the validity of our approach to resolve the inherent limitation of MEMS/NEMS switches in terms of switching speed versus pull-in voltage. Chapter 5 demonstrates the fabrication and characteristics of pure SWNT thin film based 3-terminal MEMS switches. Chapter 6 presents the simulation results in terms of device size and actuating electrode and compares with theoretical models. Chapter 7 summarizes the work and provides recommendations on future research direction.

CHAPTER 2. KEY PARAMETERS AND THEIR THEORETICAL MODELS OF ELECTROSTATIC MEMS/NEMS SWITCHES

2.1. Introduction

In this chapter, the key parameters and their theoretical models of the electromechanical switches are discussed. Especially, the spring constant model for the free-standing fixed-fixed beam could be used to extract the Young's modulus of the SWNT by AFM measurement [63] as well as to estimate pull-in voltages. The switching speed model is obtained by solving Bernoulli-Euler beam equation [64] and general motion equation based on the d'Alembert's principle [20].

2.2. Governing Forces in MEMS/NEMS Switching Operation.

The electrostatic MEMS/NEMS switches are operated by the electrostatic force when applying a potential difference between a movable/suspended beam and a fixed electrode (or multiple electrodes). In addition to the electrostatic force, the van der Waals (vdW) force and short range forces may attract the movable/suspended beam down to the fixed electrode(s) or another movable/suspended beam. The vdW force originates from the correlation of fluctuating higher order electrostatic moments between two charge distributions [65]. The vdW force is attractive and the interaction energy varies with separation as the inverse sixth power of separation in the range of separations relevant to

the MEMS/NEMS switches [66]. The attractive part of the short range force originates from a coupling between the tube and the contact when the electronic wave functions overlap [65]. Therefore, both forces may be negligible for the MEMS/NEMS switches with larger than 10nm of air-gap [65].

To turn on the MEMS/NEMS switches, the electrostatic force and other forces should overcome the elastic force of the movable/suspended beam $\left(F_{elastic} < F_{electrostatic} + F_{vdW} + F_{short\,range}\right)$ so that the movable beam is collapsed down to the fixed electrode [20, 65]. This turn-on switching is mechanically done, which results in abrupt transition from OFF-state to ON-state. In addition, the required electric voltage for this transition is called with "Pull-in voltage", which will be discussed in next section. Therefore, the MEMS/NEMS switches could provide almost off-leakage free and abrupt switching characteristics, which would be preferable to low power applications.

However, the MEMS/NEMS switches may not be turned off promptly in case that the vdW and short range attractive forces are sufficiently large enough to hold the movable beam down, even though the electrostatic potential on the actuator electrode is decreased below "Pull-in voltage (V_{pi})" to turn off (or even at 0V). It is due to the non-negligible vdW and short range forces induced by a few sub-nanometer range of small separation between movable and fixed electrodes. Therefore, the movable beam could be returned back to the original place only if the elastic restoring force would be bigger than other forces $\left(F_{elastic} > F_{electrostatic} + F_{vdW} + F_{short\,range}\right)$. It is so called "Pull-out voltage (V_{po})", which is a forced voltage on the actuator(s) when the movable beam returns back to the original position. This V_{po} may be affected by the spring constant of

movable beam, contact area, electrode surface roughness and the species of interacting atoms, etc [65]. In case of a soft beam with low stiffness and/or large contact area, the movable beam may not return back to the original position, but just stick to the fixed electrode, which is so called as "Stiction". This is a seriously problematic issue in the MEMS/NEMS switches. To prevent the stiction, the high spring constant of movable beam would be preferable, however, which results in high V_{pi}. From the design stage, the device structures and materials for the movable beam should be carefully determined. For this work, we only focus on the basic understanding of pull-in operation. Therefore, the vdW and short range force are not discussed furthermore.

2.3. Key Parameters and Their Theoretical Models

In this section, several key parameters of MEMS/NEMS switches and their theoretical models are introduced, which are spring constant of fixed-fixed beam, pull-in voltage, fundamental resonant frequency and switching speed. Finally, a basic requirement to ensure reliable operation will be discussed.

2.3.1. Spring Constant (*k*) of Fixed-Fixed Beam

In the MEMS/NEMS switches, the elastic fore is determined by Young's modulus and dimensions of the movable beam, which could be simply expressed as a spring constant. In this section, the spring constant models for 2-terminal and 3-terminal are introduced.

2.3.1.1. Case I : Two-terminal Fixed-Fixed Switch

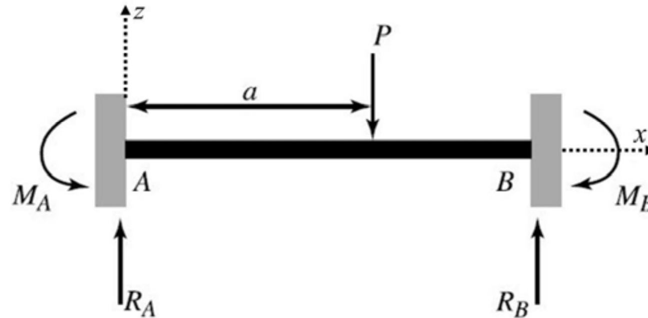


Figure 2.1: Fixed–fixed beam with concentrated vertical load P ; Reproduced from [20].

The first step to understand the mechanical operation of NEMS/MEMS switches is to derive the spring constant of the fixed-fixed beam or cantilever beam [67]. In this section, the spring constant of the fixed-fixed beam is discussed, which will be used to extract Young's modulus of the aligned-composite SWNT beam with AFM measurement. If the switching operation is limited to small deflections, the mechanical behavior can be modeled using a linear spring constant, k (N/m). Then an external force, F (N), on the fixed-fixed beam can be obtained using $F=k\Delta z$, where Δz is defined as beam deflection. The spring constant of a fixed-fixed beam can be largely modeled in two parts. One part ($k_{stiffness}$) is due to its stiffness which accounts for the material characteristics such as Young's modulus (E) and the moment of inertia(I). The other part ($k_{biaxial\ stress}$) is due to the biaxial residual stress(σ) within the beam, which is a result of the fabrication process [20]. Figure 2.1 shows the schematic of fixed-fixed beam with concentrated vertical load P and the expression for the spring constant is found from the deflection versus load

position given by [68]

$$EI\frac{d^2z}{dx^2} = M_A + R_A x\,, \qquad for\; x \le a \tag{2.1}$$

$$z = \frac{M_A x^2}{2EI} + \frac{R_A x^3}{6EI}\,, \qquad for\; x \le a \tag{2.2}$$

$$M_A = -\frac{Pa}{l^2}(l-a)^2 \tag{2.3}$$

$$R_A = \frac{P}{l^3}(l-a)^2(l+2a) \tag{2.4}$$

where l is the length of the beam, M_A (N·m) is the reaction moment at the left end, and R_A (N) is the vertical reaction at the left end. *"z"* is the beam deflection length at point a. For a rectangular cross section, the moment of inertia, I, is given by $I = wt^3/12$, where w is the width and t is the thickness of the beam [20]. For our 2-terminal device, the load is evenly distributed over the center portion of a fixed-fixed beam as below Figure 2.2, where ξ is the load per unit length.

Therefore, we can determine the spring constant by calculating the deflection of the beam at the center with substituting $x = l/2$ into the beam deflection equation "z" [20].

$$z = \frac{2}{EI}\int_{l/2}^{x}\frac{\xi}{48}(l^3 - 6l^2a + 9la^2 - 4a^3)da$$

$$= -\frac{\xi}{24EI}\left[x^4 - 3lx^3 + 3l^2x^2 - l^3x + \frac{l^4}{16}\right] \tag{2.5}$$

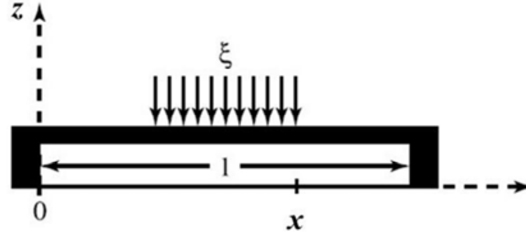


Figure 2.2: Fixed–fixed beam with the force, $P = 2\xi(x - l/2)$, evenly distributed about the center of the beam ; Reproduced from [20].

Using the evenly distributed load over the center portion of a fixed-fixed beam defined as $P = 2\xi(x - l/2)$, the spring constant can be derived by dividing the load by the beam deflection length as below.

$$k_{stiffness} = -\frac{P}{z} = \frac{2\xi\left(x - \frac{l}{2}\right)}{\frac{\xi}{24EI}\left[x^4 - 3lx^3 + 3l^2x^2 - l^3x + \frac{l^4}{16}\right]}$$

$$= 4Ewt^3 \frac{(x - l/2)}{\frac{1}{8}[(x - l/2)(8x^3 - 20lx^2 + 14l^2x - l^3)]}$$

$$= 32Ew\left(\frac{t}{l}\right)^3 \frac{1}{8(x/l)^3 - 20(x/l)^2 + 14(x/l) - 1} \quad (2.6)$$

In case of a concentrated load at the center of the beam, the spring constant can be found by substituting $x = l/2$ from the Eq.(2.6) [20].

$$k_{stiffness} = 16Ew\left(\frac{t}{l}\right)^3, \quad (2.7)$$

where E, w, t and l are Young's modulus, width, thickness and length of the free-standing beam, respectively.

The part of the spring constant due to the biaxial residual stress within the beam is

derived from modeling the beam as a stretched wire for tensile stress and it is given as below [20].

$$k_{biaxial\ stress_tensile} = 4\sigma(1-\upsilon)w\left(\frac{t}{l}\right), \tag{2.8}$$

where σ, υ, w, t, and l are the biaxial residual stress, Poission's ratio, width, thickness and length of the beam, respectively.

However, in case that the biaxial residual stress is compressive stress, this approach is not valid any more but the primary concern with compressive stress is that the beam tends to be buckled. Due to the stiffness of the beam, a certain amount of compressive stress can be withstood before buckling occurs and this stress known as the "Critical stress" for a fixed-fixed beam is given as below [20].

$$\sigma_{cr} = \frac{\pi^2 E t^2}{3l^2(1-\upsilon)}. \tag{2.9}$$

Using this critical stress, the spring constant due to compressive stress could be rewritten by

$$k_{biaxial\ stress_compressive} = \frac{4}{3}\pi^2 wE\left(\frac{t}{l}\right)^3. \tag{2.10}$$

Therefore, the total spring constant can be expressed as below [20].

$$k = k_{stiffness} + k_{biaxial\ stress} \tag{2.11}$$

$$= \begin{cases} 16Ew\left(\frac{t}{l}\right)^3 + 4\sigma(1-\upsilon)w\left(\frac{t}{l}\right), for\ Tensile\ stress \\ 16Ew\left(\frac{t}{l}\right)^3 + \frac{4}{3}\pi^2 Ew\left(\frac{t}{l}\right)^3, for\ compressive\ stress \end{cases}$$

where E, σ, υ, w, t, and l are Young's modulus, biaxial residual stress, Poission's ratio, width, thickness and length of the beam, respectively.

2.3.1.2. Case II : Three-terminal Fixed-Fixed Switch

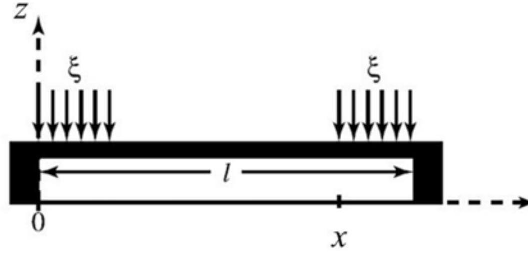


Figure 2.3: Fixed–fixed beam with the force, $P=2\xi(l-x)$, evenly distributed along the ends of the beam; Reduced from [20].

In considering both gates are biased, the spring constant (k) of 3-terminal switch can be estimated by evaluating the integral in the equation 2.5 from x to l with the force, $P = 2\xi(l - x)$, evenly distributed along the ends of the beam, as shown in Figure 2.3. In our 3-terminal device, the load is forced at the $x = {}^{4l}/_{5}$. Therefore, the equation is modified as below [20]

$$k_{3-terminal} = \left[4Ew\left(\frac{t}{l}\right)^3 \frac{1}{\left(\frac{x}{l}\right)\left(1-\left(\frac{x}{l}\right)\right)^2} \right]_{x=\frac{4l}{5}}$$

$$= 125Ew\left(\frac{t}{l}\right)^3 \qquad (2.12)$$

2.3.2. Pull-In Voltage

2.3.2.1. Case I : Two-terminal Fixed-Fixed Switch

The classical closed-form pull-in voltage model can be derived from fixed-fixed beam structure under concentrated load as shown in Figure 2.4. When a voltage is applied between a fixed–fixed beam and the pull-down electrode, an electrostatic force, F_e, is induced on the beam as shown in Figure 2.4. In order to approximate this force, the beam over the pull-down electrode is modeled as a parallel-plate capacitor [20]. This approximation provides a good understanding of how electrostatic actuation works, even though the actual capacitance is about 20–40% larger due to fringing fields [3].

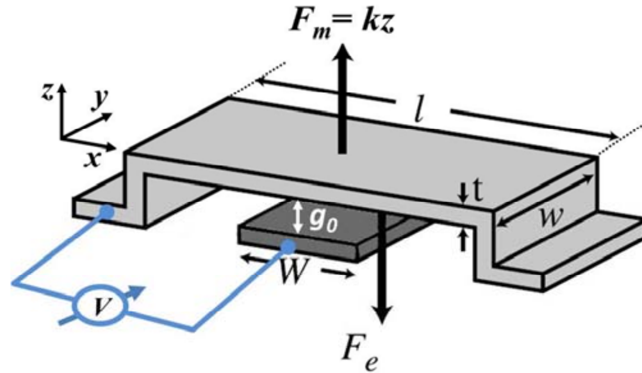


Figure 2.4: Schematic of fixed-fixed beam under concentrated load; Reproduced from [20].

The width of the beam and the pull-down electrode are w and W, respectively. The gap is position dependent, but has a value of $(g_0 - z)$ where z is the vertical deflection of the beam. Then the capacitance between the beam and bottom electrode is given by [69],

$$C(z) = \frac{\varepsilon_0 Area}{(g_0 - z)} = \frac{\varepsilon_0 wW}{(g_0 - z)}, \tag{2.13}$$

Here we assume that the gap is empty. The electrostatic force applied to the beam is found by considering the power delivered to a time dependent capacitance and is given by [67],

$$F_e = -\frac{1}{2}V^2\frac{dC(z)}{dz} = \frac{1}{2}\frac{\varepsilon_0\, wWV^2}{(g_0 - z)^2}\,, \qquad (2.14)$$

where V is the applied voltage between the beam and pull-down electrode and this electrostatic force is independent of the applied voltage polarity. In addition, the electrostatic force is approximated as being evenly distributed across the section of beam above the pull-down electrode and should be equal to the mechanical restoring force due to the stiffness of the free-standing beam ($F_m = kx$) at the static equilibrium condition [69].

$$\frac{1}{2}\frac{\varepsilon_0\, wWV^2}{(g_0 - z)^2} = kz\,, \qquad (2.15)$$

By rearranging upper equation, the equilibrium deformation can be obtained by the roots of the cubic equation below.

$$z^3 - 2g_0z^2 + g_0^2z = \frac{\varepsilon_0 wW}{2k}V^2\,, \qquad (2.16)$$

which for low voltage has a physically realistic root. As the applied bias is increased, the beam deflection increases at an increasing rate until an electrostatic instability is attained. This critical point can be simply found by solving $dV/dz = 0$, as shown below.

$$\frac{dV}{dz} = \frac{3z^2 - 4g_0z + g_0^2}{\frac{\varepsilon_0 wW}{k}V} = 0 \qquad (2.17)$$

From the upper equation, the critical deflection point is obtained by

$$z_{critical} = \frac{1}{3} g_0 \,. \tag{2.18}$$

At this critical point, the electrostatic actuation encounters positive feedback. This can be understood by considering the electrostatic force in terms of the electric field applied to the beam [20, 67]. The constant voltage source can be thought of as an infinite charge pump. As the beam is deflected the stored charge between free-standing beam and pull-down electrode is increased. As a result, the electrostatic force is increased and simultaneously the increased force decreases the beam height. In turn, the decreased beam height increases the capacitance and thus the stored charge and the electric field. Finally, from the critical point equation, equivalently, the effective air-gap at the instance of pull-in event is given by [20, 69]

$$g_{pull-in} = \frac{2}{3} g_0 \,, \tag{2.19}$$

This leads to the critical excitation voltage, the so-called pull-in voltage [20]

$$V_{PI} = \sqrt{\frac{8}{27} \frac{k}{\varepsilon_0 w W} g_0^3} \,, \tag{2.20}$$

In this equation, k is the spring constant. In the case of a concentrated load at the center of the beam [67] (as introduced in the section of 2.3.1.1)

$$k = 16 E w \left(\frac{t}{l}\right)^3 , \tag{2.21}$$

where E is Young’s modulus. Also, w, l and t are the width, length and thickness of the beam, respectively.

2.3.2.2. Case II : Three-terminal Fixed-Fixed Switch

The effective capacitance and electrostatic force between two gates and free standing beam are doubled in the equation 2.13 and 2.14. And the hafnium dioxide on gate would work as a parasitic capacitor as shown in Figure 2.6.

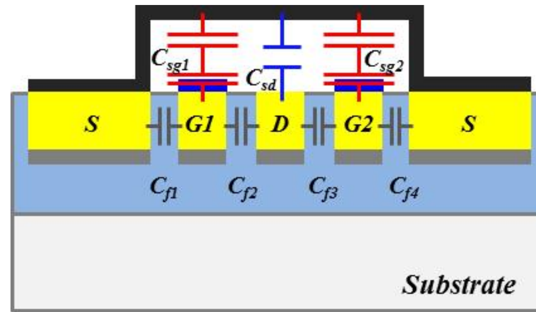


Figure 2.5: A capacitor model for our fixed–fixed beam device with small air-gap (g_0) and thin hafnium dioxide (t_d) on the gate electrodes.

The fringing capacitances (C_{f1}~C_{f4}) can be negligible due to the thick inter-dielectric layers (SiO_2) between electrodes. In the pull-in voltage modeling, the drain capacitance term could be negligible because the forced bias is very low. The equivalent capacitor between the beam and a gate electrode can be estimated by two parallel plate capacitor connected in series. One of them is due to the air-gap (g_0) and the other is due to the thin gate oxide (t_d) because the gate electrodes are insulated with 10nm thick hafnium dioxide. Assuming that the air-gap, hafnium dioxide thickness and gate overlap area for each gate are identical, the total capacitance between the beam and a gate (C_{sg1} or C_{sg2}) can be written as equation 2.22,

$$C_{sg1} = C_{sg2} = \frac{C_{g_0} C_{t_d}}{C_{g_0} + C_{t_d}} = \frac{\varepsilon_0 wW}{\left(g_0 + \frac{t_d}{\varepsilon_r}\right)}, \quad (2.22)$$

where g_0, t_d, and ε_r are the air-gap, hafnium dioxide thickness and its relative dielectric constant, respectively. When two gates are biased together, the equivalent gate capacitance is doubled in the equation 2.22. Therefore, in considering the hafnium dioxide thickness (t_d) and its relative dielectric constant (ε_r), the equation 2.15 and 2.16 become as below equation 2.23 and 2.24, respectively.

$$\frac{\varepsilon_0\, wWV^2}{(g_0 + \frac{t_d}{\varepsilon_r} - z)^2} = k_{3-terminal} z \quad (2.23)$$

$$z^3 - 2(g_0 + \frac{t_d}{\varepsilon_r})z^2 + \left(g_0 + \frac{t_d}{\varepsilon_r}\right)^2 z = \frac{\varepsilon_0 wW}{k_{3-terminal}} V^2 \quad (2.24)$$

This equation 2.24 for low voltage should have a physically realistic root. As the applied bias is increased, the beam deflection increases at an increasing rate until the electrostatic instability is attained. This critical point can be simply found by solving $dV/dz = 0$, and the equation as below.

$$\frac{dV}{dz} = \frac{3z^2 - 4(g_0 + \frac{t_d}{\varepsilon_r})z + \left(g_0 + \frac{t_d}{\varepsilon_r}\right)^2}{\frac{2\varepsilon_0 wW}{k_{3-terminal}} V} = 0 \quad (2.25)$$

From the upper equation, the critical deflection point is obtained by

$$z_{critical} = \frac{1}{3}(g_0 + \frac{t_d}{\varepsilon_r}). \quad (2.26)$$

Finally, from the critical point equation, equivalently, the effective air-gap at the instance of pull-in event is given by [20]

$$g_{pull-in} = \frac{2}{3}(g_0 + \frac{t_d}{\varepsilon_r}) \, , \tag{2.27}$$

and leading to the critical excitation voltage, so called pull-in voltage, is obtained by

$$V_{PI} = \sqrt{\frac{4}{27}\frac{k_{3-terminal}}{\varepsilon_0 wW}\left(g_0 + \frac{t_d}{\varepsilon_r}\right)^3} \, , \tag{2.28}$$

which k3-terminal is given by equation 2.12.

2.3.2.3. Consideration of Contact Surface Roughness Effect

The roughened contact surface produces a bigger surface area, in turn, larger capacitance than the case of flat surface electrodes, which results in smaller pull-in voltage. Kogut [70] reported the influence of surface topography on pull-in voltage by assuming the contact surface topology as a series of hemispheres with a radius "R" in the parallel plate capacitor as shown in Figure 2.8. When surface topography on the

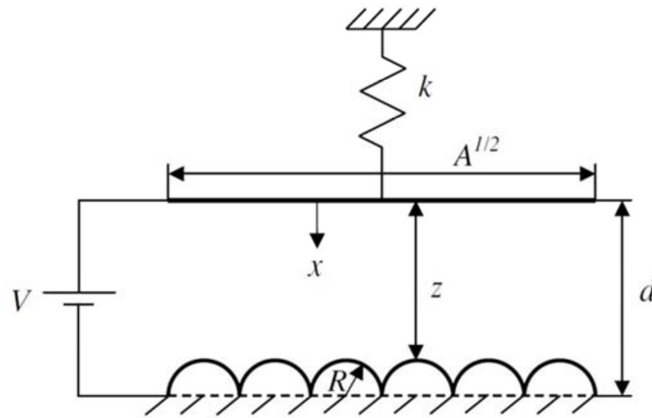


Figure 2.6: Schematic cross-section of a variable parallel-plate capacitor consisting of two smooth electrodes with surface area A and gap d. When surface topography is taken into account, equivalent roughness is modeled with hemispheres of fixed radius R uniformly distributed across the bottom electrode; Reproduced from [70].

electrodes is taken into account, analyzing the capacitance and electric field becomes a non-trivial undertaking which requires cumbersome numerical calculations [71, 72] or approximate analytical solutions by considering limit cases of the surface topography [73–76]. A common approach taken with problems involving rough surfaces is to replace the original rough surfaces with an equivalent area flat surface [77]. Roughness may be represented by the statistical approach [78] based on surface asperities of spherical summits with fixed radius and a Gaussian height distribution function. Thus, the problem is reduced to analyzing the capacitance and electric field between a sphere of radius R and a flat, as shown in Figure 2.8, where analytical solutions exist [79, 80]. The capacitance $\bar{C}$ formed between a hemisphere and a flat is given by [79].

$$\bar{C} = 2\pi\varepsilon\varepsilon_d R ln\left(1+\frac{R}{z}\right), \tag{2.29}$$

Where z is the gap between the sphere tip and the flat $z = d - R$. This analytical closed-form relationship is valid for any value of z/R, as opposed to other approximate solutions that are suitable only for a limited range of z/R [81]. The corresponding electrostatic force $\bar{F}_e$ is given by [79]

$$\bar{F}_e = \frac{\pi\varepsilon\varepsilon_d R^2 V^2}{z(z+R)}. \tag{2.30}$$

Finally, the maxim electric field E_m between a sphere and a flat surface can be written as [80]

$$E_m = 0.9\frac{V(z+R)}{zR}. \tag{2.31}$$

Kogut [70] simplified the surface topography representation by considering hemispheres of constant radius uniformly distributed across the stationary electrode. The hemisphere

radius can be related to the gold contact surface roughness [70]. For a square electrode with area A, the number of hemispheres along its side N is calculated by

$$N = \frac{\sqrt{A}}{2R} \tag{2.32}$$

and the total number of hemispheres on the electrode is N^2 [70]. Therefore, the normalized capacitance C^*defined as the ratio between the actual capacitance (C_r) from rough surfaces and the ideal capacitance from smooth electrodes (C_0) is calculated by [70]

$$C^* = \frac{C_r}{C_0} = \frac{N^2\bar{C}}{C_0} = \frac{\pi}{2}\frac{d}{R}\ln\left(\frac{1}{1 - R/d}\right). \tag{2.33}$$

This equation 2.33 depends simply on the R/d ratio. Note that the potential for divergence of equation 2.33 as this ratio approaches one is not physically meaningful as it would mean an electrical short between the upper and lower capacitor electrodes [70]. Thus, the meaningful maximum value of R/d is 0.5. In this case, the C^* approaches to 2.18. When R/d approaches zero, C^* approaches $\pi/2$, which is the ratio between the rough and flat surface areas $2\pi R^2 N^2$ and A, respectively [70]. This means that the increase in the capacitance considering surface roughness is due to both influences of larger surface area and smaller effective gap [70]. When the R/d ratio is small, the surface area term is more significant than the effective air gap term, while the opposite is true when the R/d is large [70].

The pull-in voltage of rough electrodes is calculated by solving a set of two equations below with the pull-in gap d_{pr} and voltage V_{pr} as unknowns. The set of equations represents force balance between the electrostatic and mechanical forces [70].

$$F_{er} = N\bar{F} = F_m \tag{2.34}$$

$$\frac{\mathrm{d}F_{er}}{\mathrm{d}x} = \frac{\mathrm{d}F_{er}}{\mathrm{d}x} \tag{2.35}$$

where the mechanical force is given by $F_m = kx$ and x is the displacement of the top electrode as shown in Figure 2.8 [70]. By solving this set of two equations, we get below two equations.

$$d_{pr} = \frac{d + R + \sqrt{R^2 - Rd + d^2}}{3} \tag{2.36}$$

$$V_{pr} = \sqrt{\frac{4k(d - d_{pr})(d_{pr}^2 - Rd_{pr})}{\pi\varepsilon\varepsilon_d A}} \tag{2.37}$$

Now d_{pr} and V_{pr} can be normalized with d_{p0} and V_{p0}, respectively. This yields the normalized pull-in gap d_p^* and pull-in voltage V_p^* as below [70].

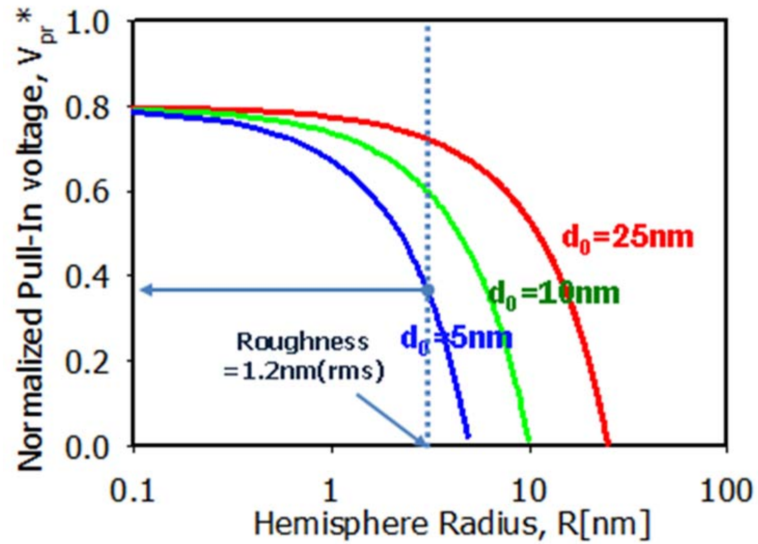


Figure 2.7: Kogut Model for surface roughness effect on pull-in voltage.

$$d_p^* = \frac{d_{pr}}{d_{p0}} = \frac{1}{2}\left[1 + \frac{R}{d} + \sqrt{\left(\frac{R}{d}\right)^2 - \frac{R}{d} + 1}\right] \tag{2.38}$$

$$V_p^* = \frac{V_{pr}}{V_{po}} = \sqrt{\frac{27}{2\pi}\frac{\left(d - d_{pr}\right)\left(d_{pr}^2 - Rd_{pr}\right)}{d^3}} \tag{2.39}$$

Using the upper two equations, Figure 2.9 shows the normalized pull-in voltage versus the hemisphere radius for various gaps. The influence of roughness to diminish the pull-in voltage becomes more significant for larger *R/d* values due to the increase in the capacitance and the associated electrostatic force [70]. Moreover, the dependency of pull-in voltage on surface roughness is increasing as fundamental air-gap is decreased.

2.3.3. Mechanical Resonance Frequency

The fundamental mechanical resonant frequency can be obtained from solving the Bernoulli-Euler beam equation assuming that the beam is uniform and made from a linear, homogeneous, isotropic elastic material [64], as shown in Figure 2.10. The deflection of the beam is $z(x, t)$ in the z direction due to total forced external force $f(x, t)$ along the beam length direction [64]. The beam has a rectangular cross section $A(x)$ with width h_y, thickness h_z, and length L.

$$\rho A(x)\frac{\partial^2 z(x,t)}{\partial t^2} + \frac{\partial^2}{\partial x^2}\left[EI(x)\frac{\partial^2 z(x,t)}{\partial t^2}\right] = f(x,t), \tag{2.40}$$

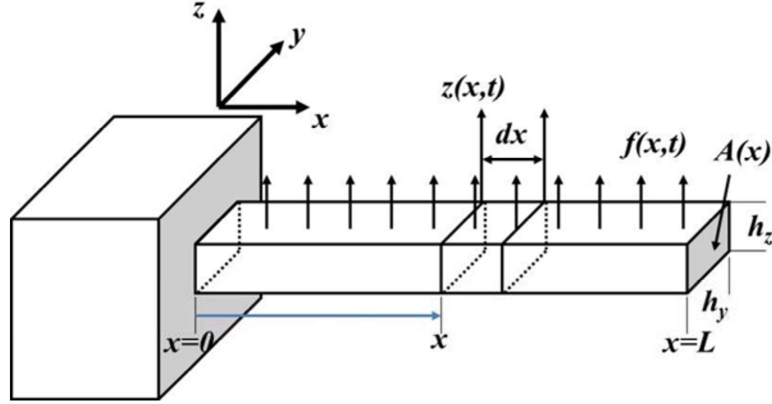


Figure 2.8: Simple beam in transverse vibration as it is deformed by a distributed force per unit length; Reproduced from [64].

where ρ, A, z, E, I and f are mass density, area, beam deflection, Young's modulus, moment of inertia for rectangular beam and applied force, respectively [64]. If no external force is applied so that $f(x,t) = 0$ and if $EI(x)$ and $A(x)$ are assumed to be constant, this equation is simplified for free vibration [64].

$$\frac{\partial^2 z(x,t)}{\partial t^2} + \frac{EI}{\rho A}\frac{\partial^4 z(x,t)}{\partial x^4} = 0 \tag{2.41}$$

The boundary conditions required to solve upper equation are obtained by examining the deflection $z(x,t)$, the slope of the deflection $\partial z(x,t)/\partial x$, the bending moment $EI\,\partial^2 z(x,t)/\partial x^2$, and the shear force $\partial[EI\partial^2 z(x,t)/\partial x^2]$ at the beam [64]. For fixed-fixed beam, the required boundary conditions are $z(0,t) = z(L,t) = 0$ and $\partial z(0,t)/\partial x = \partial z(L,t)/\partial x = 0$ [64]. In addition to satisfying four boundary conditions, the solution for free vibration can be calculated only if two initial conditions are specified [64]: the initial deflection and velocity profiles $z(x,0) = z_0(x)$ and $z_t(x,0) = \dot{z}_0(x)$. A separation-of-variables solution of the form $z(x,t) = X(x)T(t)$ is assumed and

substituted into the equation of motion,

$$\frac{EI}{\rho A}\frac{X''''(x)}{X(x)} = -\frac{\ddot{T}(t)}{T(t)} = \omega^2 \, , \tag{2.42}$$

where the partial derivatives have been replaced with total derivatives [64]. And the natural frequency ω^2 is a separation constant that comes from the temporal equation [64]:

$$\ddot{T}(t) + \omega^2 T(t) = 0 \tag{2.43}$$

This temporal equation has a solution of the form as below.

$$T(t) = Asin\omega t + Bcos\omega t \tag{2.44}$$

And the special equation is given by

$$X''''(x) - \frac{\rho A \omega^2}{EI} X(x) = 0\,. \tag{2.45}$$

By defining $\beta^4 = \rho A \omega^2 / EI$ and assuming a solution of the form $Ae^{\sigma x}$, the general solution can be calculated to be of the form [64]

$$X(x) = a_1 sin\beta x + a_2 cos\beta x + a_3 sinh\beta x + a_4 cosh\beta x \tag{2.46}$$

To derive the natural frequency(ω), we need to use four boundary conditions for fixed-fixed beam as mentioned before such that the deflection and its slope at both ends(x=0 and x=L) should be zero [64]. These four boundary conditions yield four equations in the four unknown coefficients of $a_1, a_2, a_3,$ and a_4.

$$X(0) = a_2 + a_4 = 0 \tag{2.47}$$

$$X'(0) = \beta(a_1 + a_3) = 0 \tag{2.48}$$

$$X(L) = a_1 sin\beta L + a_2 cos\beta L + a_3 sinh\beta L + a_4 cosh\beta L = 0 \tag{2.49}$$

$$X'(L) = a_1 \beta cos\beta L - a_2 \beta sin\beta L + a_3 \beta cosh\beta L + a_4 \beta sihh\beta L = 0 \tag{2.50}$$

These can be written as the single vector equation

$$\begin{bmatrix} 0 & 1 & 0 & 1 \\ \beta & 0 & \beta & 0 \\ sin\beta L & cos\beta L & sinh\beta L & cosh\beta L \\ \beta cos\beta L & -\beta sin\beta L & \beta cosh\beta L & \beta sinh\beta L \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad (2.51)$$

This vector equation can have a non-trivial solution for the vector $\vec{a} = [a_1 \quad a_2 \quad a_3 \quad a_4]^T$ only if the determinant of the coefficient vector is zero.

$$\det\left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ \beta & 0 & \beta & 0 \\ sin\beta L & cos\beta L & sinh\beta L & cosh\beta L \\ \beta cos\beta L & -\beta sin\beta L & \beta cosh\beta L & \beta sinh\beta L \end{bmatrix}\right) = 0 \qquad (2.52)$$

Then we get the characteristic equation, $cos\beta L \cdot cosh\beta L = 1$ and this equation has an infinite number of choices for β, denoted β_n. The fundamental resonant frequency is found as below equation 2.53 using $\beta_1 L = 4.73004074$ from [64].

$$f_0 = \frac{\omega_0}{2\pi} \cong 1.0279\left(\frac{t}{L^2}\right)\sqrt{\frac{E}{\rho}} \qquad (2.53)$$

2.3.4. Switching Speed

Theoretically, the switching time for a 2-terminal fixed-fixed beam can be obtained using d'Alembert's principle [82]. The general equation of motion is given by

$$m\frac{d^2z}{dt^2} + b\frac{dz}{dt} + kz = f_{ext} \qquad (2.54)$$

where z is the bridge displacement, m is the bridge mass, b is the damping coefficient, k is the spring constant, and f_{ext} is an external force. The switching time depends strongly on the applied voltage since the larger the voltage that is applied, the stronger the electrostatic force. A closed-form solution for the switching time can be obtained for inertia limited systems, which is for beams with a small damping coefficient and large

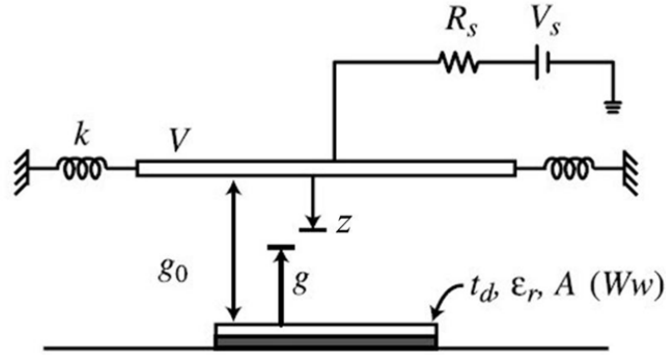


Figure 2.9: The 1-D MEMS beam model and its coordinate system; Reproduced from [20].

quality factor [20]. Then the upper equation of motion becomes as below, assuming the damping coefficient as zero. (Figure 2.9)

$$m\frac{d^2z}{dt^2} + kz = -\frac{1}{2}\frac{\varepsilon_0 A V_s^2}{g_0^2} = f_{ext}(0) \tag{2.55}$$

where the force is taken to be constant and equal to the initial applied force $(f'_{ext}(0) = 0)$ [20]. Using Laplace transformation and the initial conditions$(x(0) = x'(0) = 0)$, the upper equation can be rewritten by

$$Z(s) = \frac{f_{ext}(0)}{s(ms^2 + k)} = \frac{1}{m}\frac{f_{ext}(0)}{s(s^2 + \frac{k}{m})}\,. \tag{2.56}$$

This X(s) equation can be converted to time domain using inverse Laplace transformation table [83] as below

$$\mathrm{z(t)} = \frac{f_{ext}(0)}{k}\left[1 - \cos\sqrt{\frac{k}{m}}t\right] \cong \frac{f_{ext}(0)}{2m}t^2. \tag{2.57}$$

The switching is done at the time when the free-standing beam is contacted to the bottom electrode as $z(t_s) = -g_0$. Since the switching time is very small, the equation 2.57 uses a Taylor series expansion to provide a simple form. Using the pull-in voltage (V_p), as explained in the section 2.3.2.1, the switching time can be rewritten by

$$t_s \cong \sqrt{\frac{27}{2}\frac{V_p}{V_s\omega_0}}, \quad (2.58)$$

where $V_s, V_p,$ and, ω_0 are a supply voltage, pull-in voltage and mechanical resonant frequency, respectively [20]. From this equation, we can see that the switching time is inversely proportional to the mechanical resonant frequency of fixed-fixed beam.

2.5. Summary

In this chapter, the key parameters and their models of the electrostatic MEMS/NEMS switches were introduced based on the relationships between elastic and electrostatic forces while switching operations. Using spring constant models, Young's modulus of a movable and suspended beam can be estimated through the AFM [63] or tribonanoindentation [84]. In the chapters 4 and 5, the measured pull-in voltages and switching speed will be compared with each theoretical model.

CHAPTER 3: LITERATURE REVIEW OF CARBON NANTUBE BASED THIN FILM DEPOSITION TECHNIQUES

3.1. Overview

Carbon nanotubes (CNTs) have been studied extensively due to their unique electrical [85-89], mechanical [90-96], chemical [97-98], optical [99-103] and thermal properties [104-105]. However, the current carrying capacity of individual CNTs is too small to meet the requirements of nanoelectronics or micro- and nanoelectromechanical systems (MEMS and NEMS) [56, 57]. It is possible to mitigate these limitations simply by forming a CNT thin film, which can also be produced by in situ or post-growth techniques. CNTs can be randomly distributed or well aligned in the film depending on the deposition process. Randomly distributed CNT film can be obtained by drop casting [106-108], spin coating [109-113], vacuum filtration [114-120], transfer printing [121-123], spraying [124-129], chemical vapor deposition (CVD) [130-134], electrophoretic deposition (EPD) [135-148], or layer-by-layer (LbL) self-assembly process [149-162]. Aligned CNT films can be deposited through patterned CVD growth [163-168], fluidic channeling [169-176] and dielectrophoresis [177-180]. The fundamental concepts, along with the merits and demerits of each technique, are introduced in the following sections.

3.2. Randomly Distributed Carbon Nanotube Films

CNTs can be distributed randomly or directionally in the film depending on the deposition process. In this section, several techniques for randomly distributed CNT films are briefly introduced and their merits and demerits are discussed.

3.2.1. Drop Casting

This process is the easiest technique for randomly distributed CNT film deposition [106-108] with a solution-based deposition process. In this process, CNTs are adhered on a surface through the drying of the dispersion. Typically, one drop of dispersion is deposited on the surface and the solvent or deionized water is evaporated

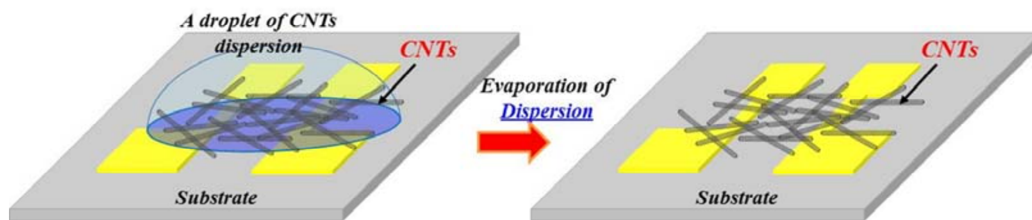


Figure 3.1: Drop casting on a substrate; Reproduced from [106].

with a heat using a hot plate or oven as shown in Figure 3.1, often accompanied by a vacuum [107]. Ko *et al* [56] demonstrated a modified drop casting by tilting the substrate while evaporating dispersion as shown in Figure 3.2. Prior to drop casting, the substrate surface was functionalized with a NH_2-terminated self-assembled monolayer (SAM) to increase the adsorption of CNTs on the substrate [56]. Purification of single-wall carbon nanotubes synthesized by arc-discharge (Carbon Solutions, Inc) was performed by mild

air oxidation (350 °C, 2 hours), followed by a 6 M hydrochloric acid washing for 2 h. A stable dispersion of CNTs was achieved by dissolving purified CNTs in 1% aqueous sodium dodecyl sulfate (SDS) solution by sonication for 2 hours. Centrifugation (18,000 rpm, 1 hour) was used to remove agglomerates [56]. For this process, an appropriate amount of SWNT solution was spread on the tilted substrate and left without perturbation inside a sealed container [56]. As the solvent evaporated, the liquid-solid-air contact line swept down the surface, accumulating highly concentrated solution in the vicinity and leaving a dense CNT layer behind the receding line [56]. CNTs in the film are randomly distributed as shown in right image of Figure 3.2. However, stains from the dispersion may remain at the edge of the evaporated dispersion. This can limit the concentration of the CNT dispersion, which may make it hard to get a densely packed film [56].

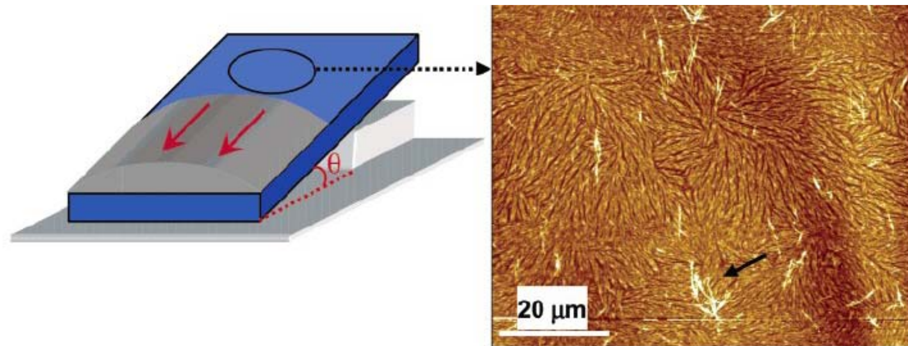


Figure 3.2: (Left) Tilted-drop casting process, (Right) AFM image of CNTs film; Reproduced from [56].

3.2.2. Spin Coating

Spin coating has been recognized as the most promising process for mass production and industrialization of SWCNT thin films because of the uniformity of the film, ease of thickness control, short coating time, low-temperature fabrication, and high reproducibility [112]. In this process, it is critical to use the appropriate surfactant for dispersion of SWCNTs in solvent. The most conventional surfactants used for dispersion

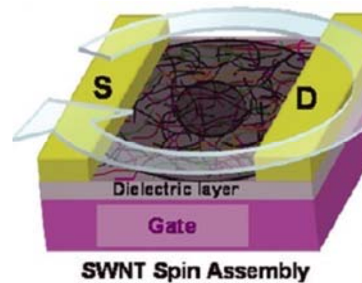


Figure 3.3: Spin coating process for CNTs film; Reproduced from [110].

of SWCNTs are sodium dodecyl sulfate (SDS) and sodium dodecylbenzene sulfonate (SDBS) [112, 181]. Although these surfactants have been well-known to disperse SWCNTs effectively in aqueous media for spin coating, the strong charge repulsion between complexes of SWCNT/surfactant due to ionic groups of surfactant inhibits deposition of SWCNTs on the substrate. This results in a limited thickness of the SWCNT film [112, 182]. To overcome the problem, three types of spin coating processes have been proposed: repeated spin coating of SWCNT solution without surfactant [181], dual spinning method [183] which exclude the repulsive effect of surfactant during the spin coating process, and the use of a non-ionic surfactant [112,

182]. Although dpin coating provides some control of the deposited film thickness by changing spin speed and concentration of CNT dispersion, this control is quite limited. Thus, spin coating is not a good choice to get a conformal film with a well-controlled thickness,

3.2.3. Vacuum Filtration

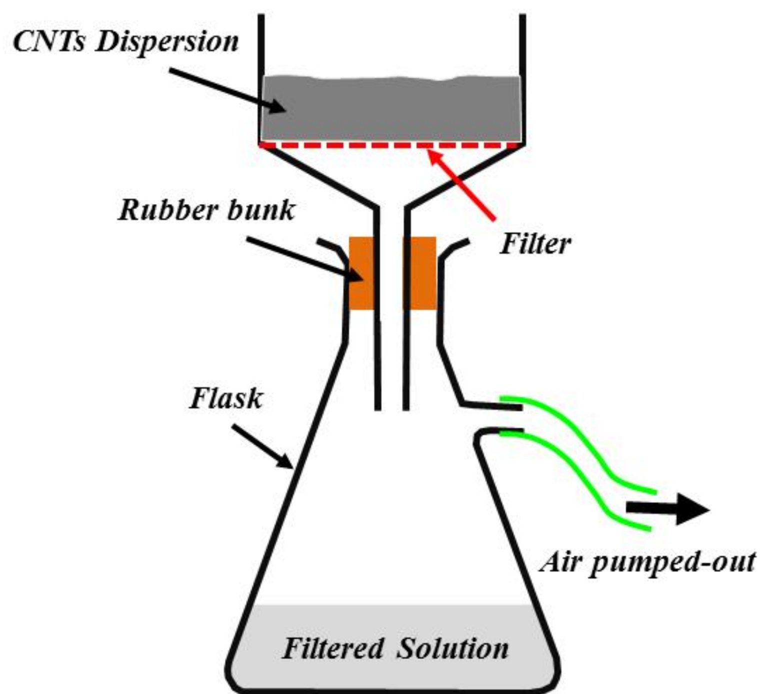


Figure 3.4: Apparatus for vacuum filtration method; Reproduced from [184].

The vacuum filtration method involves vacuum filtering a dilute suspension of nanotubes in a solvent over a porous filtration membrane. As the solvent diffuses through the pores, the nanotubes are trapped on the surface of the filter, forming an

interconnected network. The density of this network (nanotubes/area) can be controlled with high precision by simply controlling the volume of dilute suspension filtered through a membrane [114-120]. This method also has the benefit that the speed of the vacuum filtering process does not allow for tube flocculation, creating optically homogeneous films [115]. Another factor that aids in homogeneity is that the denser regions block fluid flow through the filter [115]. The filtration method is inexpensive, scalable to large areas, and allows for the transfer of the film to other surfaces by membrane dissolution [114-117]. However, it is unclear whether the filtration method is suitable for fabrication of transparent conducting CNT electrodes since concurrent optimization of sheet resistance and visible transmittance would not be easy [181]. Moreover, the filtration method requires extra process steps to remove surfactants such as sodium dodecylsulfate (SDS) and to transfer CNT films to desired substrates [181]

3.2.4. Transfer Printing

The transfer printing is a dry method to transfer the CNTs from a filter membrane prepared by vacuum filtration method [122, 123] or a stamping substrate such as poly(dimethysiloxane) (PDMS) prepared by spin coating method [111, 121] to target substrates. This dry-transfer approach, initially developed by Zhou *et al*. [123] uses an adhesive, soft, and flat PDMS stamp to peel the SWNT film off of the filtration membrane and then release it onto a desired substrate, as shown in Figure 3.5 [122]. This transfer printing requires mild heating during contact (100 °C, 1 min) to improve the adhesion of the target substrates. The relief process on the stamps, however, may disrupt

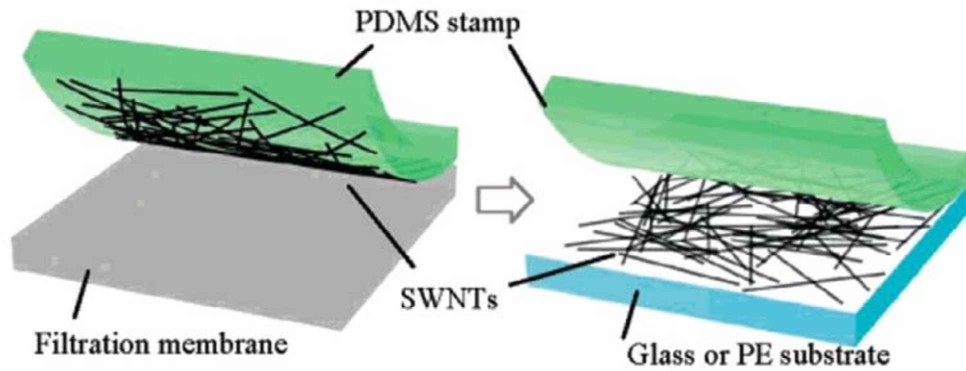


Figure 3.5: Schematic of a transfer printing process; Reproduced from [122].

a precise placement on the surface to some extent and decrease the level of coverage uniformity [111].

3.2.5. Spraying

Spray coating is a very simple method for depositing CNTs over a substrate [124-129, 184]. It is done through the use of a commercial air brush pistol with a CNT dispersion. After preparation of the CNT dispersion, the suspension is then directly sprayed onto the substrates while keeping the substrate on a hot plate as shown in Figure 3.6. A proper temperature (typically 80 to 200˚C depending on the substrate on solvent) must be selected to accelerate the drying of the small droplets on surface [125, 126]. This heating procedure would be extremely helpful when spraying over large areas. However, large droplet formation is very difficult to avoid in this process, even though the CNT dispersion was extensively centrifuged. This may be due to droplet-droplet collisions in the aerosol. Large droplets can degrade the mechanical properties of CNT films. Lateral thickness variations caused by large droplets would be extremely troublesome when the

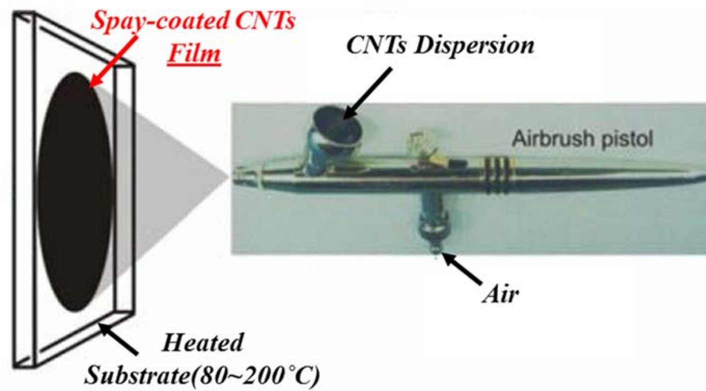


Figure 3.6: Schematic of a spaying process; Reproduced from [184].

resultant CNT film is being used as a free standing beam material for MEMS/NEMS switch applications. To improve this limitation, Kim *et al*. [125] introduced the electrostatic spray deposition technique, but it has a basic limitation that the target substrate should be metallic.

3.2.6. Chemical Vapor Deposition

Chemical vapor deposition (CVD) proceeds by decomposing a carbonaceous gas (carbon monoxide [185], hydrocarbons such as methane [186], ethylene [187], acetylene [188], methanol [189] or benzene [190]) in a tube reactor at temperatures ranging from 550 to 750˚C on a finely dispersed catalyst such as Fe, Ni, and Co. Figure 3.7 illustrates a classic CVD system [191]. The hydrocarbon enters the reactor along with an inert carrier gas. As the hydrocarbon decomposes, carbon deposits onto the catalyst, which is supported by a material such as alumina. Carbon has a low solubility in these metals at high temperatures and thus the carbon will precipitate to form nanotubes [192]. CNT

growth in CVD can be split into two basic types depending on the location of the catalyst, so-called base growth mode, and tip growth mode [193]. All of them can be split into bulk carbon diffusion and surface carbon diffusion models.

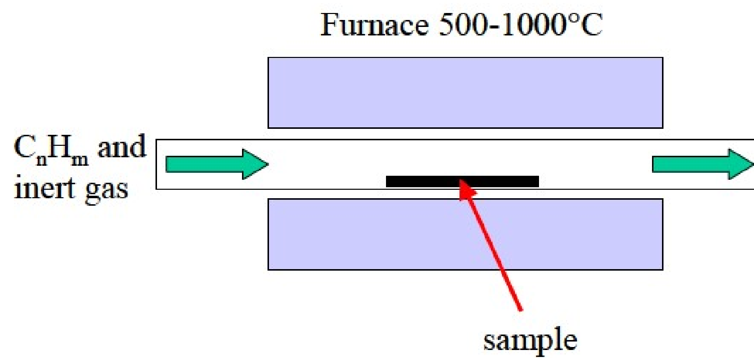


Figure 3.7: Schematic of a classic CNT CVD reactor; Reproduced from [191].

In substrate growth, the catalyst nanoparticles or metal precursors are deposited either on a substrate such as SiO_2 or on a high surface area powder before growth [193], as shown in Figure 3.8(a). In the gas phase growth, catalyst formation and nanotube growth occur in mid-air [193], as shown in Figure 3.8(b). Various CVD techniques for the carbon nanotubes synthesis have been developed, such as plasma enhanced CVD [194], thermal chemical CVD [195], alcohol catalytic CVD [196], vapor phase growth [197], aero gel-supported CVD [198] and laser assisted CVD [199].

This is the most controllable method for producing CNTs suitable for mass production and large-area deposition [200]. Thus, CVD yields the most important technique for potential industrial applications. However, most of CVD techniques use

high temperature precluding many substrates of interest. With the PECVD approach it is possible to deposit CNTs below 350°C [194]. The CVD method had the disadvantages of low yield and amorphous-carbon impurities, which limited its application for large-scale production of nanotubes [198].

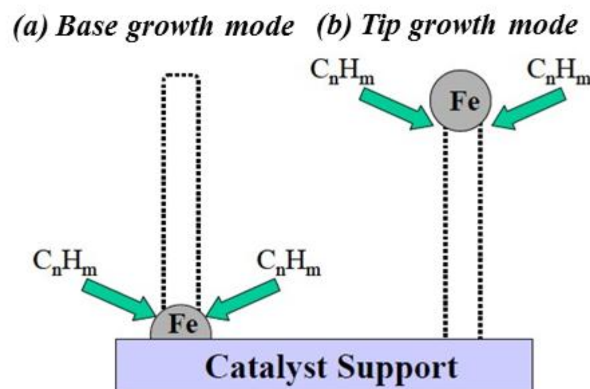


Figure 3.8: Schematic of two general CNT CVD growth modes; Reproduced from [193].

3.2.7. Electrophoretic deposition

Electrophoretic deposition (EPD) [135] fundamentally consists of two processes such as electrophoresis and deposition. In the first step, material (particles) suspended in a liquid are forced to move towards an electrode by applying an electric field. In the second step, the particles collect at the electrode and form a consistent deposit [201]. EPD has several advantages when using particulate suspensions to generate films and coatings, as well as laminar ceramic composites and functionally graded materials [202-204]. Most of all, EPD is not only a very cost-effective method usually requiring simple

equipment as shown in Figure 3.9, but also offers the possibility of forming monolithic or composite coatings with complex shapes and/or surface patterns [135].

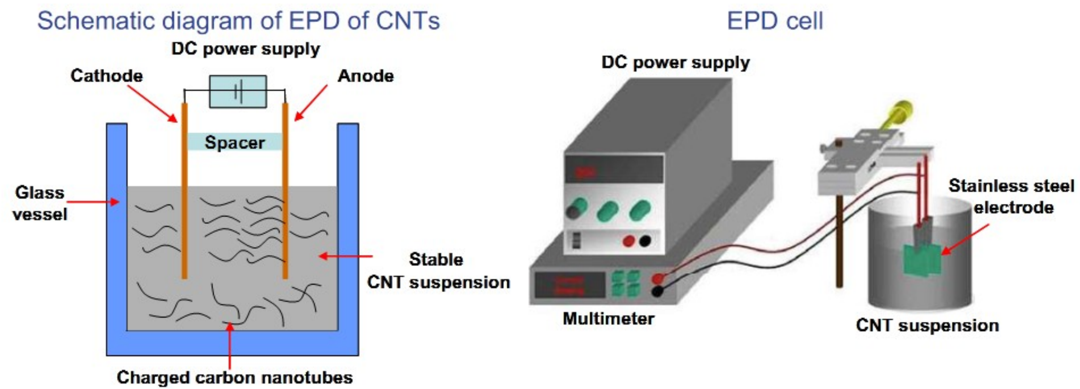


Figure 3.9: Schematic of anodic-electrophoretic deposition of CNTs, showing the cell (left) and the overall set-up (right); Reproduced from [135].

Additionally, EPD can reduce the processing time dramatically, as much as two orders of magnitude shorter than other suspension-based processes such as drop casting [135, 205]. The deposition rate is also relevant for controlling the compositional profile of functionally graded materials deposited by EPD [206]. Preparation of a stable dispersion of CNTs in a suitable solvent is a necessary prerequisite for successful EPD of CNT films. The most common strategy is the production of an electrostatically stabilized dispersion, which, in general terms, requires the preparation of a solvent medium in which the particles have a high zeta-potential, while keeping the ionic conductivity of the suspensions low [139]. As reported in the literature, several types of solvents have been used to prepare CNT suspensions for EPD, including distilled water [207], mixtures of

acetone and ethanol [208], and pure organic solvents such as ethanol [209], isopropyl alcohol (IPA) [210], n-pentanol [211], ethyl alcohol [212], tetrahydrofuran (THF) [213], dimethlyformamide (DMF) [214] and deionized water with pyrrole [215]. Moreover, the presence of charger salts can play an important role in improving the adhesion of CNTs to substrates and in increasing the deposition rate in the EPD process [212, 220–222]. Salts can also contribute to the stability of the suspensions by associating a charge with the CNT surface in suitable solvents. The migration direction of CNTs in suspension during EPD is controlled by the surface charge. For example, oxidized nanotubes are typically negatively charged and attracted to the positive electrode (anode) [218]. More subtle control can be achieved by using different types of charger salts. A variety of salts have been adopted in CNT suspensions including quaternary ammonium salts [213, 223–224], benzalkonium chloride [220], $NiCl_2$ [221], $Mg(NO_3)_2$ [211,216], $MgCl_2$ [212] and NaOH [217]. CNTs deposited on the anode when benzalkonium chloride or metal charger salts were used, while the deposition on the negative electrode (cathode) was observed for quaternary ammonium salt and sodium hydroxide containing suspensions [139]. The effect can be understood in terms of ion adsorption. For example, Mg_2^+ ions are adsorbed by the suspended CNTs, encouraging the formation of an electric double layer [217]. The migration and resultant deposition of CNTs under the influence of a DC field has been attributed to preferential absorption of ions in the solution by the nanotubes [217]. Therefore, a suitable charger salt can be selected depending on whether deposition is required at the anode or the cathode [139]. A summary of the electrophoretic deposition parameters used in the literature, including electrode materials, deposition

time, deposition voltage and electrode separation, is listed in Table 3.1. The deposition rate and yield of EPD method depends primarily on the applied electric field because for a CNT dispersion with constant resistivity, a higher electric field is expected to increase the CNT velocity toward the oppositely biased electrode [135].

Electrode properties	EPD parameters Constant			Reference
	Constant voltage	Deposition time	Inter-electrode Spacing	
Stainless steel (1 · 1· 0.2 cm3)	5–50 V	0.5–10 min	20 mm	[140]
Aminopropoxysilane (APS) pretreated Optically Transparent Electrodes (OTEs)	500 V & 50 V	1min & 2min	~6mm	[132]
Carbon Fibre paper Electrodes (CFE) (2.25 · 2.25 · 0.6 cm3)	~ 40 V	–	~ 5mm	[145]
Aluminium electrodes	45V	–	50mm	[131]
Metal electrodes	45V	–	50mm	[130]
Titanium (1 x 1cm^2)electrodes	–	–	–	[142]
Cathode: Glass plate (1 cm · 0.5 cm) with ITO coating Anode: Glass plate (1 cm · 0.5 cm) with aluminium coating	100–200 V	–	18, 11, 3 & 1 mm	[143]
Silicon wafer (cathode) and stainless steel mesh as an anode	30–600 V	–	20 mm	[138]
Stainless steel mesh (cathode) and a gated triode structure formed on a glass substrate (anode)	30–200 V	–	–	[137]
Indium tin oxide (ITO) coated glass	–	–	–	[134]
Conducting glass electrodes, optically transparent electrode (OTE)	100 V	–	5mm	[146]
Conducting glass electrodes, optically transparent electrode (OTE)	<100 V & >100 V	2–3 min	5mm	[135]
Polyimide film coated with titanium (cathode) and stainless steel (an	100 V	1–2 min	–	[144]
Stainless steel	20 V	–	10 mm	[139]
Patterned metal substrates	10–50 V	–	–	[141]
Patterned dielectric substrate with 1 lm thick polysilane film coating	2000 V/cm	A few min	–	[132]
Nickel and stainless steel substrates or metal-plated glass plate	200–300 V	2min	20 mm	[147]
Nickel substrates (10 · 10 mm2)etched with 20%HNO3 for 10 min	20 V	5min	–	[136]

Table 3.1: Overview of EPD for CNTs parameters reported in previous literatures; Reproduced from [139].

However, when using deionizeddwater as a solvent for the CNT dispersion, water may lead to hydrogen (cathode) and oxygen (anode) gas evolution via electrolysis at high electric field (>35 V/cm) and at long deposition times [135]. Gas evolution may produce bubbles in the dispersion and influence the morphology of the CNT film by trapping bubbles within the deposited CNT network [208]. Therefore, the electric field should be controlled to minimize this problem.

3.2.8. Layer-by-Layer Self-Assembly

The sequential adsorption of oppositely charged colloids was initially reported in a seminal paper in 1966 by Iler [226]. The electrostatic layer-by-layer (LbL) self-assembly was subsequently rediscovered in the nineties by Decher and his coworkers [149], who extended it to the preparation of more complicated multilayers. They demonstrated an oppositely charged polyelectrolyte multilayer film with molecular-level thickness controllability [149], can be obtained by repetitive dipping into oppositely charged solutions with intermediate washing and drying [227], as shown in Figure 3.10. The positively charged substrate is immersed into a polyanionic solution, followed by the rinsing with deioninzed water and drying with nitrogen (N_2).

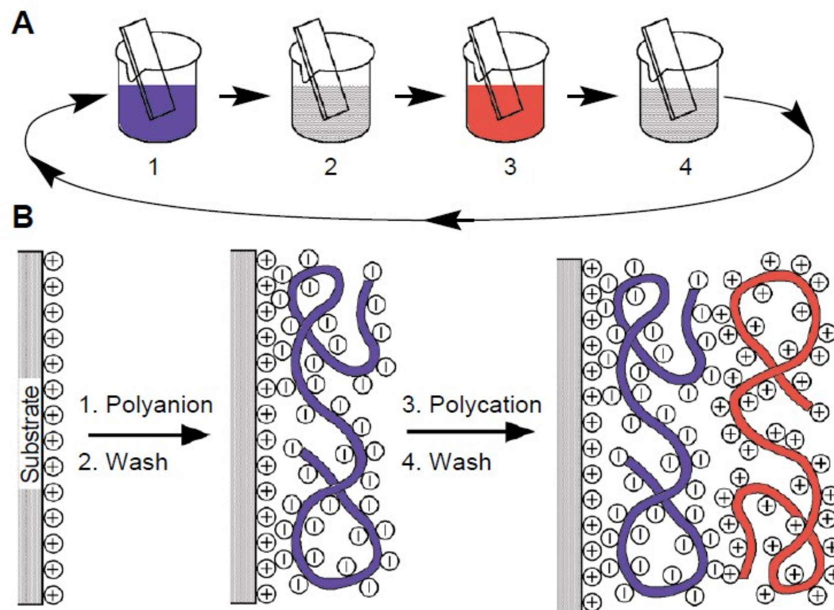


Figure 3.10: (a) Schematic of LbL self-assembly process, (b) Simplified molecular picture of the first two adsorption steps; Reproduced from [227].

Then its surface becomes negatively charged and attracts cationic ions in next step, which results in the cationic species being assembled onto the polyanion-covered surface. This process is repeated until target thickness is reached. Because the process only involves adsorption from solution, there are in principle no restrictions with respect to substrate size and topology. The film prepared by LbL is thermodynamically stable, versatile, simple, low-cost, and defect-free [227]. Due to these merits, LbL self-assembly process has been adopted for a variety of applications such as biomolecules [228], nanoparticles/nanocomposites [229], and CNTs [150-162]. For LbL deposition of CNT films, CNTs should be wrapped with charged molecules [230] or functionalized because CNTs precipitate into ropes or bundles due to strong van der Waals interactions between CNTs [231]. Various surface modifications have been used to disperse CNTs, including chemical functionalization using strong acids [232-233]. Charged molecules can be adsorbed on the CNT, when CNT is dispersed in a polyelectrolyte solution such as poly sodium 4-styrenesulfonate (PSS) and polydiallyldimethylammonium (PDDA) [230, 234]. NaBr salt in a polyelectrolyte solution can be used to control the morphology of the films [230]. This deposition method suggests a means of reducing the agglomeration of CNTs and of building up ordered three-dimensional arrays by using a polyelectrolyte such as PSS and PDDA [230, 234]. However, LbL self-assembly process may still be prone to produce agglomerates and precipitates during deposition, which result in poor mechanical and electrical properties of the multilayered CNT film [235]. Moreover, the multilayers by LbL self-assembly process are formed by electrostatic bonding force, which is weaker than covalent bonding force [236]. Bruening et al. used poly(allylamine hydrochloride)

(PAH) and poly(acrylic acid) (PAA) to construct multilayer films. The subsequent heat treatment induced the formation of amide bonds, through which the films were cross-linked and their stability improved greatly [237].

3.3. Aligned Carbon Nanotube Films

Highly dense, randomly oriented CNTs have been used recently as effective semiconducting layers for thin-film transistors. However, the inter-nanotube contact resistance of many overlapping tubes limited the full exploitation of the intrinsic high mobility [57, 238-241]. To improve these electrical properties, CNTs should be aligned parallel to the direction of current flow [56]. In this section, three techniques for forming aligned CNT films are discussed: chemical vapor deposition with a patterned catalyst [163-168], fluidic alignment [169-176] and dielectrophoresis [177-180].

3.3.1. Chemical Vapor Deposition with Patterned Catalyst

The controlled synthesis of aligned SWNTs arrays on substrates is useful making integrated carbon nanotube-based circuits [242-246] and especially high frequency electronics [247-253]. Advances in the growth of horizontally aligned and densely packed SWNTs arrays have recently been achieved on single-crystal quartz wafers by chemical vapor deposition (CVD) of ethanol [254, 255]. For the synthesis of aligned arrays of SWNTs on substrates, pre-designed catalyst structures and the immobilization of the catalysts are both very important. Especially on quartz wafers Rogers' group found

that if catalysts are not patterned on the surface, a large number of curved or random SWNTs are produced by the CVD growth [168, 256]. Thus, an easy strategy to build catalyst structures on the surface of wafers is an important goal in the area of SWNT growth [248, 255].

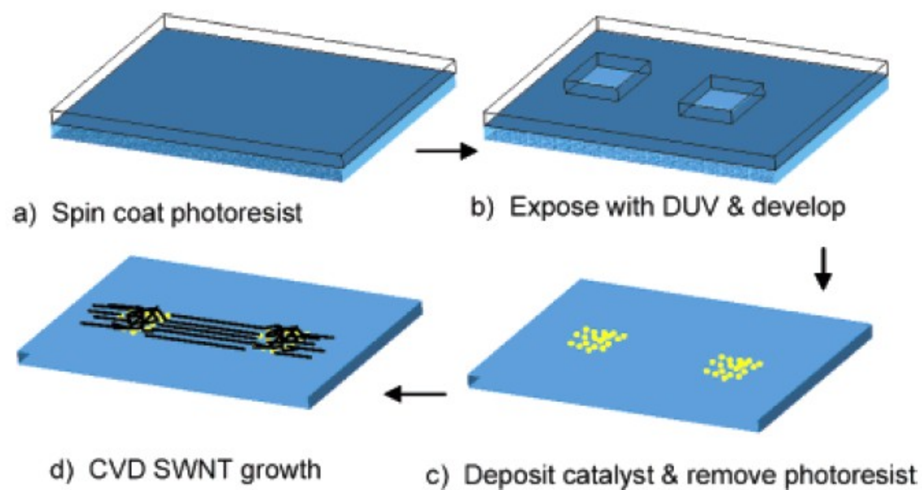


Figure 3.11: Schematic of the steps for generating self-aligned patterns of dense arrays and random networks of single-walled carbon nanotubes; Reproduced from [167].

Kocabas *et al*. [167] used spin-coating of ferritin diluted 1:20 (v/v) with deionized water as a catalyst on photoresist and the exposed regions of the quartz by photolithography as shown in Figure 3.11. Washing with acetone, isopropyl alcohol, and DI water removed the PMMA and produced a bare quartz substrate with catalyst located in regions corresponding to the patterned openings in the PMMA. The ferritin was sufficiently well adhered to the quartz that most or all of it remained during the steps to remove the PMMA. Depending on the deposition conditions, catalyst concentration, and spin speed, the number of catalyst sites per unit area in these regions was controlled.

Then the CVD growth of SWNTs was done. High-density random networks of SWNTs formed in the regions of the catalyst. However, well aligned SWNTs emerged from these regions along directions of preferred growth on the quartz, as shown in Figure 3.12.

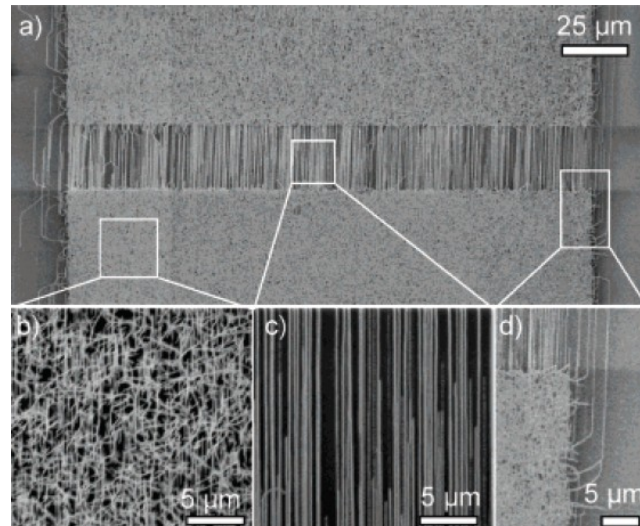


Figure 3.12: SEM images of SWNT grown using catalyst particles patternedin two square regions to form an arrangement of SWNTs, (a) SWNT network "electrodes" connected by a channel of aligned SWNTs. (b) Electrode and (c) channel regions; Reproduced from [167].

Zhou *et al.*[168] directly doped $FeCl_3$ into Shipley-1827 photoresist or polyvinylpyrrolidone in a methanol solution as the catalytic precursors. Due to the presence of the polymers, we can design perfect patterns of catalysts on a wafer scale using only a simple photolithography technique or using a PDMS stamp through the microcontact printing technique. Moreover, we found both Shipley 1827 photoresist and PVP to be effective in contributing to the formation of mono-dispersed catalyst nanoparticles as well as hindering them from aggregating on the substrate during the CVD process. Especially, for the former, very uniform and well aligned arrays of SWNTs

were synthesized with an average density of ~10 SWNTs/μm and lengths of up to a millimeter.

Although the patterned catalyst base CVD technique can produce almost perfectly aligned and densely packed CNT film, as introduced in the conventional CVD technique, it requires a high temperature process, which may limit its application for substrates with low melting or transition temperature, as well as exact positioning of the catalyst [198].

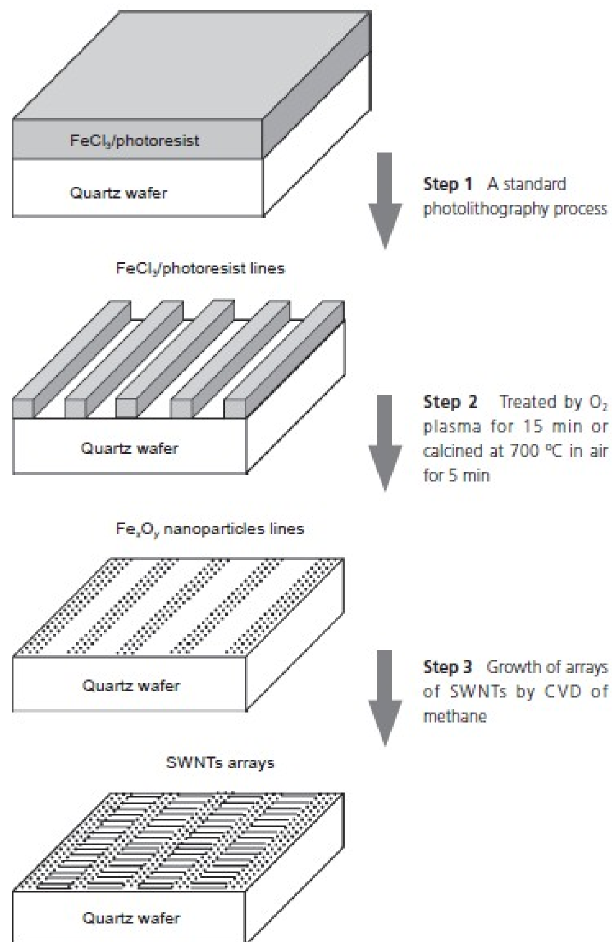


Figure 3.13: Schematic of the procedures for patterning catalyst lines by simple photolithography and the growth of arrays of SWNTs on quartz wafers; Reproduced from [168].

3.3.2. Fluidic Alignment

Most of the solution-based CNT deposition processes produce a random network of CNTs, which has an inferior current drivability to well aligned network of CNTs due to their large inter-CNT contact resistance [169-170]. Based on fluidic alignment techniques, several approaches have been reported such as the capillary-driven flow method of CNT dispersion through PDMS micro-channels [169-170, 173, 257-258], and the liquid-crystal processing methods using a CNT dispersion with surfactant in deionized water [56, 174, 176] or with liquid crystals as a solvent and director [171-172].

Lieber *et al* [257] used microfluidic alignment using PDMS channels combined with serial electron beam patterning to produce aligned and relatively rigid nanowires. Several groups have also used microfluidic flow to pattern and align SWNTs [169-170, 173], as shown in Figure 3.14.

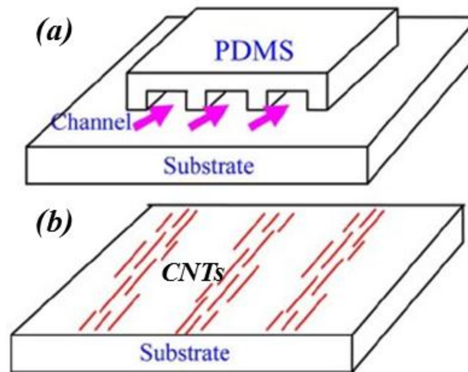


Figure 3.14: Schematic of the fluidic alignment process. (a) PDMS mold placed on the substrate surface to form parallel capillary channels as indicated by the pink arrows. SWNT suspension is placed at the entrances of the channels. (b) Aligned CNTs arrays remained on the substrate, after drying and removal of the mold; Reproduced from [170].

Park *et al* [258] recently demonstrated a method for in situ flocculation and patterning of SWNTs by inter-diffusion of two laminar liquid streams in micron-scale fluidic channels. However, the CNT patterns obtained are typically of micron scale. Ko *et al* [56] have used patterns of hydrophilic and hydrophobic areas to control the deposition of SWNT suspension on the hydrophilic areas with pattern widths of several microns. These hydrophilic/hydrophobic regions are typically patterned by contact printing which cannot easily achieve nanoscale dimensions [56], as shown in Figure 3.15. Furthermore, the flexible SWNTs deposited tend to curl and are of high areal density. Others [259-260] have used gas flow to align SWNTs on a flat Si wafer surface. Although they were able to align many tubes and the SWNTs deposited were relatively long (around 5–10 μm), gas flow by itself has difficulty in controlling the width and pitch of SWNT patterns and for low areal density SWNTs deposited over micron-scale rather than nanoscale areas [56]. In addition, their method may not be directly applicable to the rough surfaces of wafers pre-patterned with Au electrodes which protrude from the surface [56].

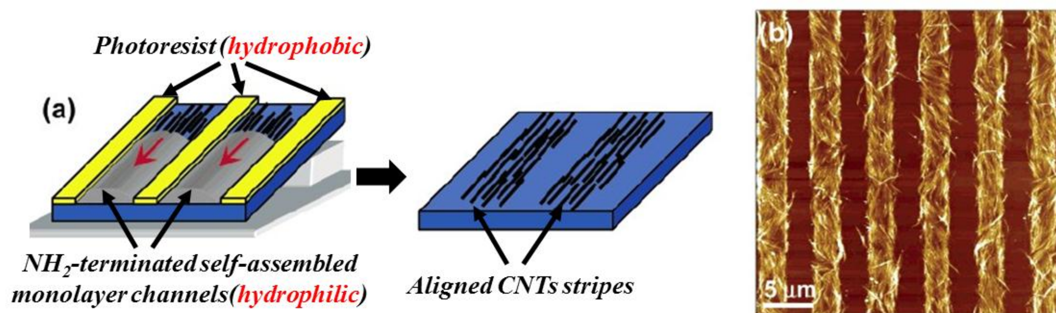


Figure 3.15: (a) Schemes for the tilted-drop fabrication of a thin film on an amine-terminated SAM surface micropatterned with photoresist polymer stripes. (b) AFM topographical images of carbon nanotube films; Reproduced from [56].

3.3.3. Dielectrophoresis

Electrophoretic deposition (EPD) techniques were reviewed in the section 3.2.7. With the EPD method, CNT films can be deposited quickly and on various kinds of conducting substrates. This method, however, produces a random network of CNTs due to its non-directional electric field on the plating electrode. Furthermore, CNTs are only deposited on the conductive substrate. Its deposition yield and rate primarily depends on the applied electric field, which is uniform between two electrodes [135].

Dielectrophoresis (DEP) is the result of the force exerted by a non-uniform electric field on the field-induced dipole moment of the polarized particle [261], as shown in Figure 3.16 [180]. In 1951, Pohl [262] reported the DEP effect for the first time including a theoretical explanation and its use for removing suspended particles from polymer solution. A comprehensive review was presented by Bruke *et al* [263].

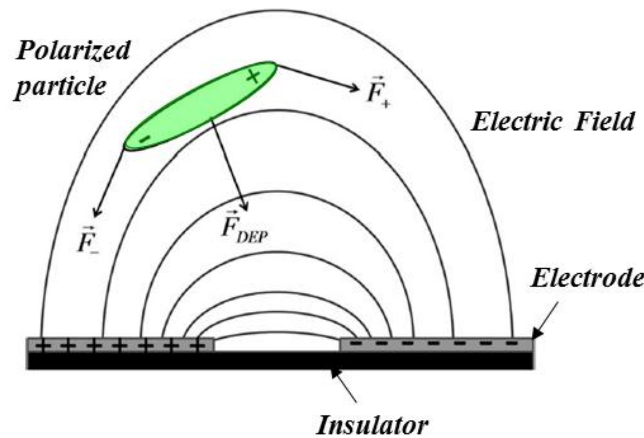


Figure 3.16: A polarized-particle modeled as a single dipole in a prolate-ellipsoid in the electric field between two charged electrodes in case that the polarization degree of the particle is larger than the medium (positive DEP force); Reproduced from [180].

In a DEP force, polarized particles move in response to an applied voltage across electrodes. The response of the material is sensitive to the sign of the applied voltage [264]. There are two different effects associated with DEP [264]. A positive DEP force occurs when the particles are more polarized than the medium, causing the polarized particles to move forward to the maximum field gradient. Negative DEP force works in the opposite direction [264]. Bruke *et al* [263] demonstrated that metallic SWNTs could be separated from the semiconducting ones due to different signs of their DEP force at high electric field frequency. However, separating particles with similar properties requires extensive optimization of the experimental parameters, such as buffer conductivity, field strength, and frequency [261]. Moreover, the film deposition by DEP is a localized event and a pair of electrodes is required for each device. This may be a hurdle to extend the process to large scale film deposition.

3.4. Summary

As reviewed in previous sections, there are a variety of CNT film deposition techniques. Each method has unique merits and de-merits. Drop casting, spin coating, vacuum filtration and spraying techniques are very simple and easy ways for CNT film deposition. In addition, they could be applied with other techniques together such as transfer printing. However, the deposited film thickness may be not easy to control [68]. CVD is a productive and conventional CMOS fabrication friendly process, but one of its concerns is the need for high temperature while the CNT film is grown. EPD is very cost

effective due to its simple set-up and short deposition time and can be used to deposit a composite film. However, it needs a conductive substrate. In the other hand, the LbL self-assembly provides tight CNT film thickness control to molecule size level and is applicable to most kinds of substrate with proper sets of functionalization and charged copolymers. The patterned catalyst CVD technique provides good alignment of CNTs between catalyst patterns during deposition, but it requires high temperature growth and exact positioning the catalysts. Fluidic alignment produces the formation of long-range ordered and dense arrays of CNTs on functionalized and/or micropatterned geometries, which is a kind of drop casting technique. However, it is not applicable to the rough surfaces of wafers pre-patterned with electrodes which may protrude from the surface. Using the DEP technique, it is possible to deposit highly ordered CNT film between two electrodes with a simple set-up and short deposition time. This requires one pair of energized electrodes per device, which may limit its applicability for large scale deposition.

Our goal is to make low power, high speed MEMS/NEMS devices with CNT thin films to reduce power dissipation in digital logic [187]. To be processed after CMOS fabrication, one of critical issues may be the process temperature during the CNT film deposition. In addition, the selected CNT film deposition process should be applicable to various kinds of substrates. In conclusion, it is believed that the LbL self-assembly, dielectrophoresis and electroplating techniques could meet most of those requirements for our application. Therefore, for this work, the LbL self-assembly and dielectrophoresis

were applied for the aligned-composite and pure SWNT thin film depositions for MEMS/NEMS switch applications, as discussed in Chapters 4 and 5, respectively.

CHAPTER 4. FABRICATION OF 2-TERMINAL NEMS SWITCHES USING ALIGNED-COMPOSITE SWNT THIN FILMS

4.1. Overview

This chapter discusses the fabrication of fixed-beam switches using an aligned composite single-walled carbon nanotube (AC-SWNT) membrane by a newly developed film density controllable dielectrophoretic self-assembly process. (This AC-SWNT film was prepared and characterized by Professor Cui's group [63]. I summarize the process here to provide context for the device fabrication sequence.) The pull-in voltage and switching delay of fixed-beam switches using this AC-SWNT membrane are discussed in this chapter.

4.2. Aligned-Composite Thin Film Preparation

4.2.1. Detailed Deposition Process [63]

The layer-by-layer (LbL) self-assembly was used to increase the SWNT density in a membrane. A variety of functional thin films can be produced using the layer-by-layer (LbL) assembly technique. Thin films are created by alternately exposing a substrate to positively- and negatively-charged molecules or particles [227]. For each step, the substrate surface is fully covered with single type of charged molecules or particles due to electrostatic repulsion force between them, which means the LbL self-assembly is a kind of self-limited process [227]. As shown in Figure 4.1, the substrate with Cr/Au

electrodes was first treated with Piranha cleaning (H_2SO_4:H_2O_2=5:1, 120˚C, 10 minutes) or O_2 plasma cleaning (100sccm, 100mT, 100W, 5 minutes) in the STS plasma etcher, to make the substrate was negatively charged [63]. Then the substrate is dipped into a poly(diallyldimethylammonium chloride) (PDDA) solution for 10 minutes and any remaining PDDA is rinsed away with deionized water. After being fully dried with a N_2 blow-off gun, the substrate is dipped into the poly(styrenesulfonate) (PSS) solution, then rinsed and dried again. In this way, a bi-layer consisting of PDDA/PSS and PDDA were LbL self-assembled on a silicon dioxide surface between two Cr/Au counter electrodes to make the surface positively charged [63].

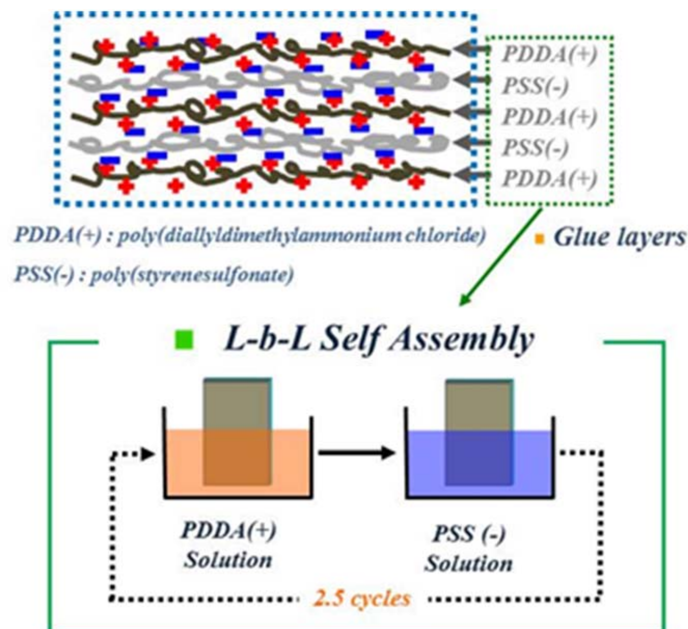


Figure 4.1: Substrate surface pre-treatment by Layer-by-Layer self-assembly with polyelectrolytes; PDDA (positively charged) and PSS (negatively charged); Reproduced from [266].

Next, a single-walled carbon nanotube (SWNT) (99% purified) water solution from Nanointegris was put in an ultrasonic bath with the chip immersed in the solution vertically, and an ac electric field was applied as shown in Figure 4.2. After the deposition the chip was rinsed in DI water followed by nitrogen blow drying [63]. During the deposition process, an analog switch circuit was applied to control the alignment and deposition of SWNT membrane between two electrodes.

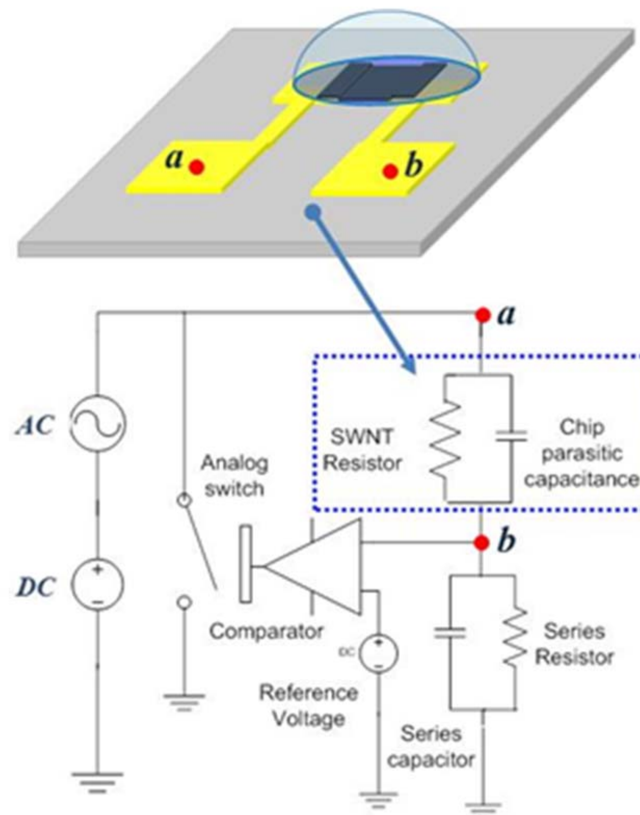


Figure 4.2: Schematic illustration of a controlling analog switch circuit; Reproduced from [63].

4.2.2. Film Characteristics

4.2.2.1. Structural Observations

In the conventional SWNT thin film made with a layer-by-layer self-assembly process, the SWNT bundles are randomly distributed. Figure 4.3 (a) shows the SEM image from SWNT composite film made of two (PDDA/PSS) cycles, followed by five (SWNT/PDDA) bilayers. The dielectrophoretic self-assembly process clearly produces well-aligned SWNT film. As explained in 4.2.1, when the substrate is connected to ac power source, the carbon nanotubes are aligned with the electric field between two electrodes resulting in well-aligned carbon nanotube thin film as shown in Figure 4.3 (b). These films are far lower resistivity than nonaligned LbL composite films, making them suitable for switch fabrication.

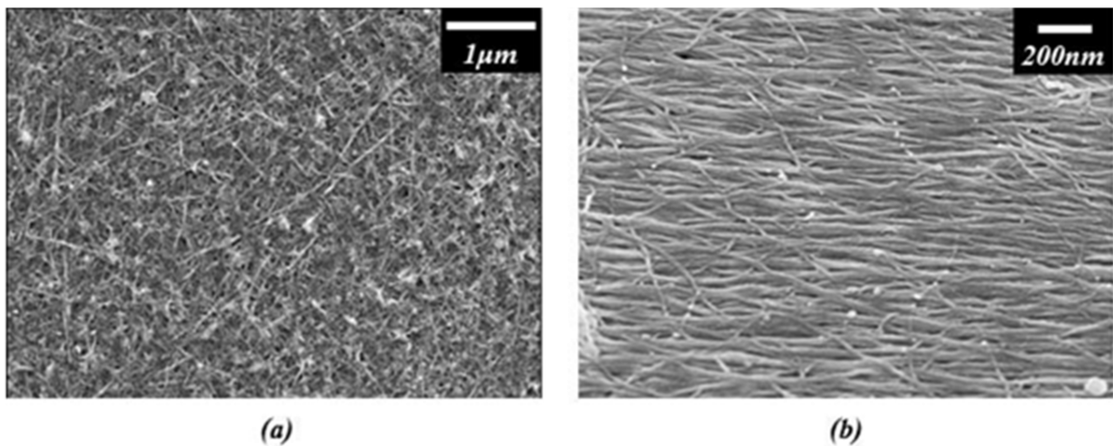


Figure 4.3: Comparison of carbon nanotubes distribution in (a) not-aligned composite SWNT thin film with layer-by-layer self-assembly, and (b) well-aligned composite SWNT thin film with dielectrophoretic self-assembly (Courtesy of Prof. Cui group).

4.2.2.2. Mechanical Properties

Young's modulus of the aligned-composite SWNT film was estimated by Prof. Cui's group through the AFM measurement on the free-standing fixed-fixed beam using the spring constant model for fixed-fixed beam. The detailed measurement techniques and related theories are reported in [63]. Estimated Young's modulus of the SWNT membrane was ranged from 350 to 830 GPa due to the thickness variation (15~20nm). This result is higher than the report Young's modulus (100 GPa) of SWNT ropes [267] and is far larger than the reported Young's modulus (35 GPa) of SWNT layer-by-Layer film by Mamedov *et al* [268]. The electric field induced SWNT condensation is one possible reason resulting in a higher Young's modulus. For example, Mureau *et al*. [269] demonstrated that SWNTs could be concentrated and trapped by an electric field through fluorescence imaging.

Discussion

Estimating Young's modulus using AFM measurement is based on ignoring the biaxial stress effect on the spring constant of the free-standing beam. However, this may produce the overestimated stiffness of aligned-composite SWNT film. Even if we assumed the intrinsic residual stress of aligned-composite SWNT film is negligible in the spring constant measurement [63], the film could be affected by the extrinsic residual stress. In our process, the α-Si layer was used as a sacrificial layer, which is strongly compressive material (~ −300MPa) and so a tensile stress could be set up in the free-standing film after α-Si layer is removed. From SEM images and measured pull-in

voltages, the released beams are a bit sagged downward and it turns out the free-standing beam has a tensile stress. However, we cannot apply the biaxial stress model introduced in [20] because it is not an isotropic material inherently. Therefore, other approaches would be required to estimate the Young's modulus more accurately considering the biaxial stresses in the film, for example, the interferometric technique [270] and for the shear modulus from the fundamental resonant frequency measurement [271].

4.2.2.3. Electrical Properties

The I-V properties of three types of SWNT beams with the same contact area and different dimensions were tested as shown in Figure 4.4. The width of the SWNT beams is 3 μm and the length of the beams are 150, 350, and 500 nm respectively, and the average thickness is measured by AFM as about 17 nm.

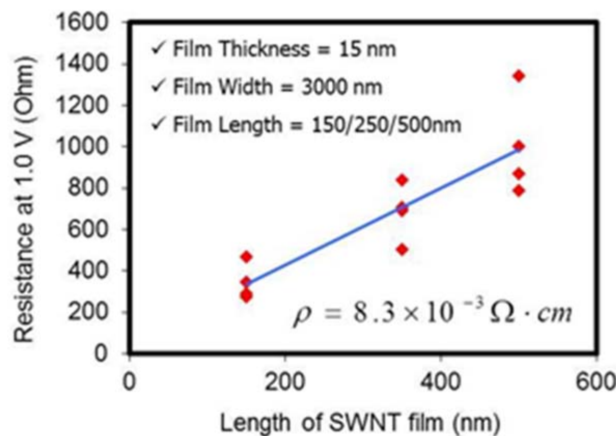


Figure 4.4: Resistance of SWNT beams depending on their different lengths; Reproduced from [63].

At a bias of 1.0 V, the resistance R of the film is found to fit the equation: R= (1.9 Ω/nm) × L + 54Ω, where L is the length of the beam with the unit of nanometer. From the slope of the equation and the dimensions of the film, the resistivity of the SWNT film is about 8.3×10^{-3} Ω·cm [63].

Discussion

Thess *et al* [272] calculated the resistivity of ropes of metallic SWNTs to be in an order of 10^{-4} Ω·cm at 300 K, and the resistivity of SWNTs in the alignment direction by a direct printing is 2.32×10^{-3} Ω·m [273]. Li *et al* [274] reported an aligned Hipco SWNT film with a resistance of more than 25 times higher than the aligned laser-ablation SWNT film by the layer-by-layer assembly.

Xue *et al* [266] reported the resistivity of randomly distributed SWNTs-PDDA composite thin film was measured about 0.2 Ω·cm. The randomly distributed SWNTs are big obstacle for current flow. Especially, this would become worse when each SWNT is short and sandwiched with a copolymer. The PDDA is very highly resistive like as a kind of insulating materials and their film is basically multi-layer PDDA/SWNT stack. In our approach, only one PDDA layer was applied and the SWNTs in the film were aligned in parallel direction with current flow by dielectrophoresis. As a result, we could get about 20 times smaller resistivity.

4.3. Two-Terminal Device Fabrication

Figure 4.5 (a) shows schematically the fixed-beam switch used in these experiments. It consists of three metal electrodes. The center is nominally labeled the gate.

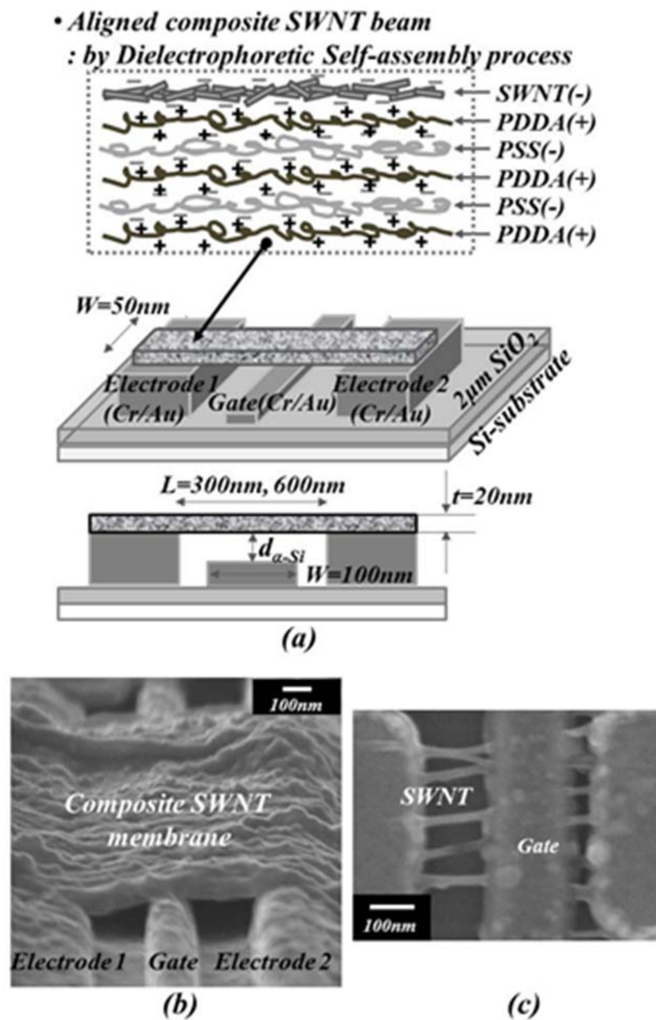


Figure 4.5: (a) top: Schematics of Layer-by-Layer self-assembled and aligned SWNT film, middle: name of each part of device and bottom: vertical dimensions of device, (b) SEM image of the fixed-beam switch, (c) SEM image of the SWNT bundles switch.

A suspended AC-SWNT membrane connects the other two electrodes as shown in Figure 4.5 (b), which would be released by etching amorphous silicon (α-Si) as a sacrificial layer. The height of gate is about 40nm less than two other electrodes. Barring beam sagging, the membrane should be suspended. The prepared switches were 50 nm wide, the gate was 100x300 nm or 100x600 nm and used a 20 nm thick membrane. For comparison, we also prepared switches made of SWNT bundles as shown in Figure 4.5 (c).

4.3.1. SWNT Thin Film Patterning Process

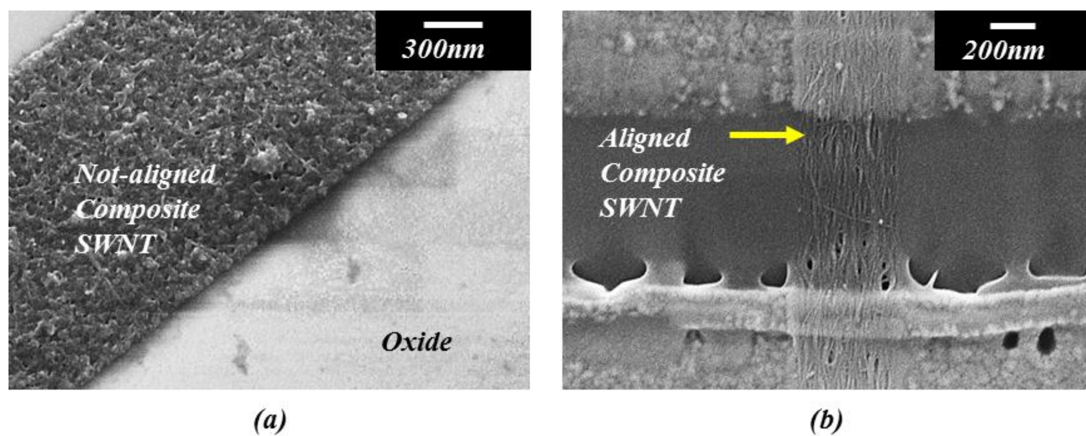


Figure 4.6: Patterned composite SWNT film by photolithography and O_2 plasma RIE etching, (a) Not-aligned composite SWNT film made of PDDA/SWNT multi-layer, (b) Aligned composite SWNT film through dielectrophoresis (Courtesy of Prof. Cui group).

To successfully fabricate a free-standing AC-SWNT membrane device, two critical processes had to be developed, patterning process of the AC-SWNT film and a stiction-free device release process. The AC-SWNT film is structurally made of multi-layer

copolymer and SWNTs stacks. Therefore, it is possible to be patterned with O_2 plasma reactive ion etch (RIE). Such a process is typically very effective for removing organic materials. Initially, etch experiments were performed with ~30nm thick not-aligned composite SWNT films. Etch conditions were a power of 100 W, a pressure of 50 mTorr, and an oxygen flow-rate of 100 sccm. The O_2 plasma RIE process worked well, as shown in Figure 4.6 (a). Moreover, this approach is directly to be extendable to AC-SWNT film patterning because the not-aligned composite film has same copolymers (PDDA, PSS) and SWNTs in its structure, as shown in Figure 4.6 (b).

4.3.2. Device Release Process

Most of the yield problems associated with MEMS devices are a result of the three dimensional nature of the surface micro-machined components. One of the most critical of these problems is "stiction" or the sticking of a mechanically "released" part to another surface [275]. This problem reduces yield and profitability of MEMS technologies.

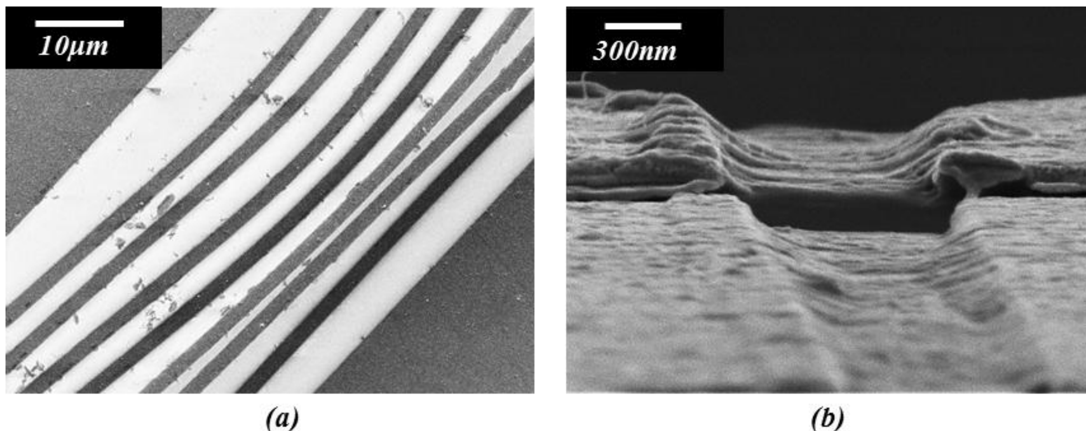


Figure 4.7: composite SWNT film collapsed after HF vapor etch of sacrificial layers (a) Not-aligned composite SWNT film with SiO_2 as a sacrificial layer, (b) Aligned composite SWNT film through dielectrophoresis with Al_2O_3 as a sacrificial layer.

Surface tension is a root causes in process induced stiction [275]. In a typical sacrificial surface micromachining process, the structural layers are separated from each other and from the substrate by sacrificial layers. These sacrificial layers are typically removed in the last step of the process by a blanket wet etch (typically an aqueous HF solution or its vapor). The structures are then rinsed and dried. The rinsing liquid, usually water, is trapped in the narrow gaps between the wafer and the suspended structure. Interfacial forces generated when the trapped capillary fluid dries can cause the microstructures to collapse and stick to the bottom substrate. Once stiction occurs in MEMS processing, it is extremely difficult to regain device functionality. Figure 4.7 shows an SEM image after SiO_2 etching with HF vapor as our initial attempts. The membranes are just collapsed to the bottom.

Supercritical CO_2 drying, sometimes referred to as critical point drying, takes advantage of the vanishing surface tension of a supercritical liquid [275]. Although critical point drying could mitigate this problem, it was not a perfect solution.

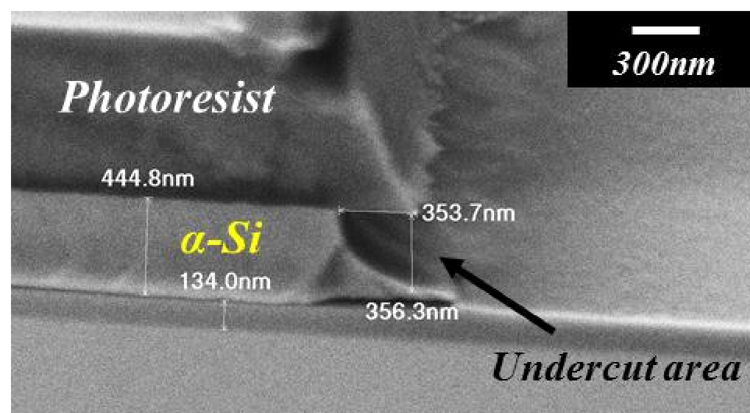


Figure 4.8: SEM image of 450nm thick α-Si deposited substrate with photoresist after removal of the α-Si.

To resolve this stiction problem, we developed a dry release process using α-Si as a sacrificial layer and removing it through an isotropic plasma etch. Figure 4.8 shows an SEM image of a 450nm thick α-Si film with the photoresist mask after an etch of the α-Si using an STS dry etcher (Model 320) with the process conditions of 50 W power, 100 mTorr pressure, and 50 sccm SF_6 flow for 1min. The undercut and vertical etching depth of α-Si are almost same as about 350nm, indicating an isotropic etch.

4.3.3. Overall Process Flow

Figure 4.9 shows the overall process steps using E-beam lithography to make the fixed-beam suspended AC-SWNT membrane switch. The Cr/Au stacked gate electrode is first formed using the Raith150 system and a lift off process on 2μm thick SiO_2. 25 nm of α-Si is deposited as a sacrificial layer by plasma enhanced chemical vapor deposition (PECVD). Two other electrodes are patterned by E-beam lithography. The thickness of α-Si layer needs to be well controlled since it determines the air gap between the AC-SWNT membrane and the gate electrode. This gap is a critical parameter that affects the overall switching characteristics. Prior to depositing the 2nd Cr/Au, the α-Si is removed by dry etching using the STS dry etch process described in the last section for 3 minutes to form anchor points for the fixed-fixed beam switch. The 2nd Cr/Au deposition and lift off processes then follow to form the other two metal electrodes. Next, the AC-SWNT membrane is deposited on the device and it is patterned by E-beam lithography and O_2 plasma etching as described in Section 4.3.1. The etch time was 3 minutes.

Finally, all of the α-Si under the patterned membrane is removed by dry etching

using a 3 minute release etch process.

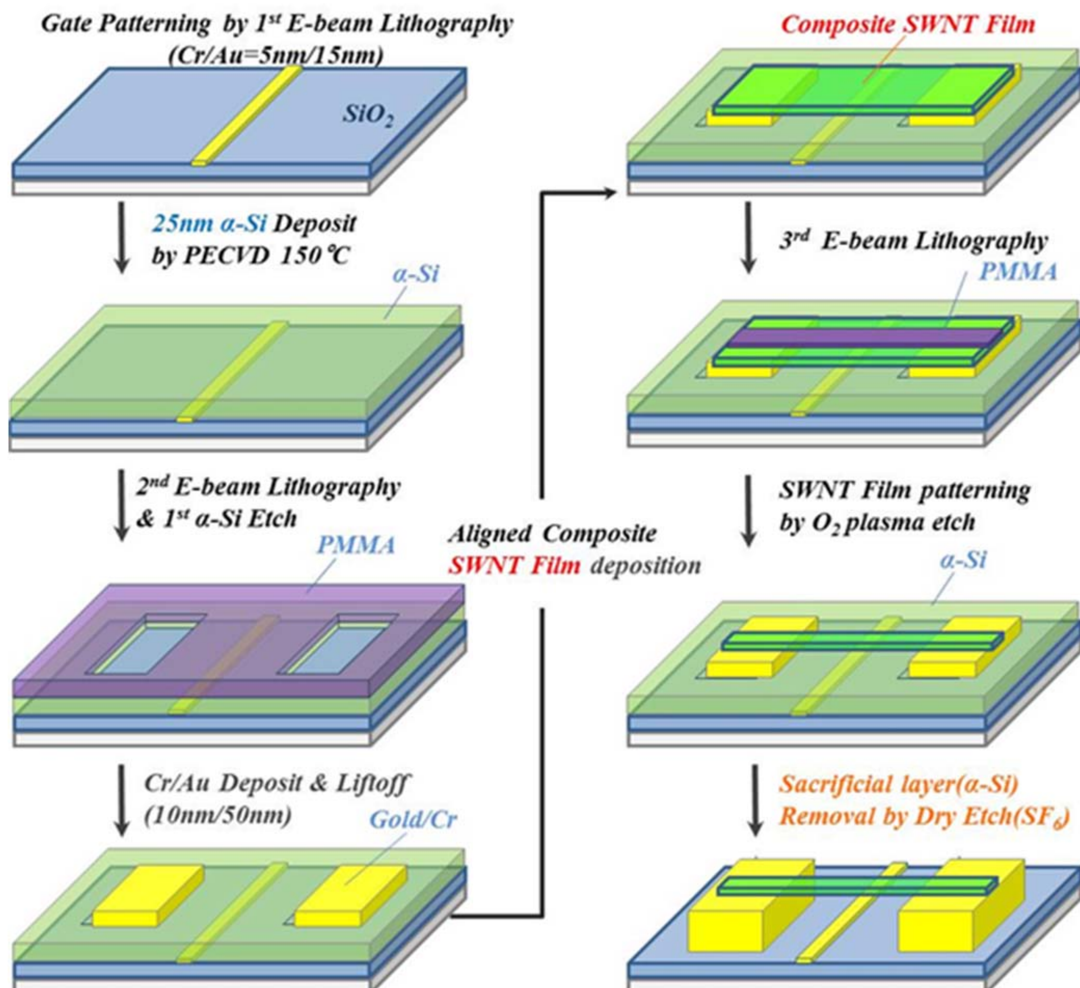


Figure 4.9: Overall process steps for 2-terminal NEMS switch with AC-SWNT membrane.

4.4. Device Characteristics

In this section, the characteristics of fabricated 2-terminal switches are discussed including pull-in voltage and switching delay. Also they are compared with theoretical models and discussed.

4.4.1. Pull-In Voltage

4.4.1.1. Measurement Set-up

The pull-in voltage was measured by applying a dc voltage between the gate and the AC-SWNT beam as shown in Figure 4.10.

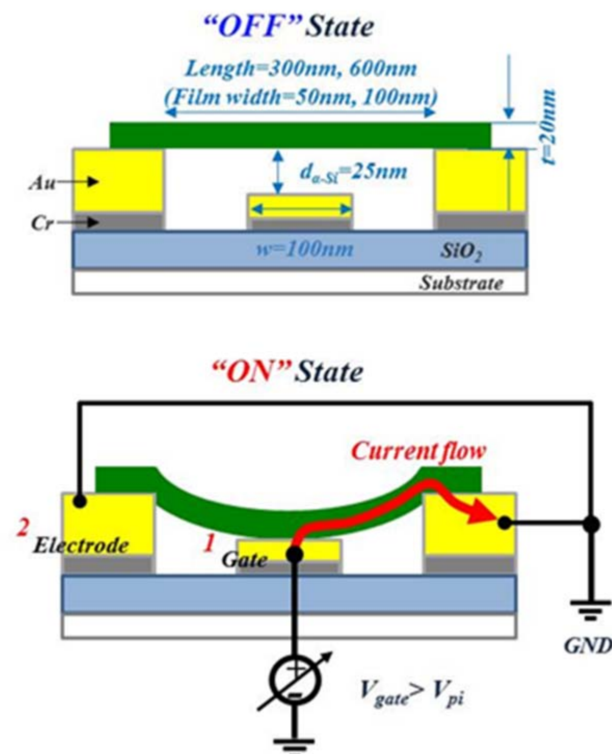


Figure 4.10: Schematic of pull-in voltage measurement set-up.

Increasing the bias voltage increases the electric charge on the AC-SWNT beam, which results in an electrostatic force between the gate and the beam. When this force is large enough to overcome the mechanical restoring force in the beam, it snaps down.

4.4.1.2. Single Beam Switch vs. Bundles Switch

Figure 4.11 shows an I-V characteristic between the gate and the two electrodes of a fixed-beam switch. When a voltage lower than 1.5 V is applied, the currents between gate and suspended AC-SWNT beam are less than a few picoamps (noise limited). When the applied voltage reaches at 3.3 V, the current suddenly increases. to ten microamps, the compliance limit for the test electronics. (The shape of the transition is discussed below.)

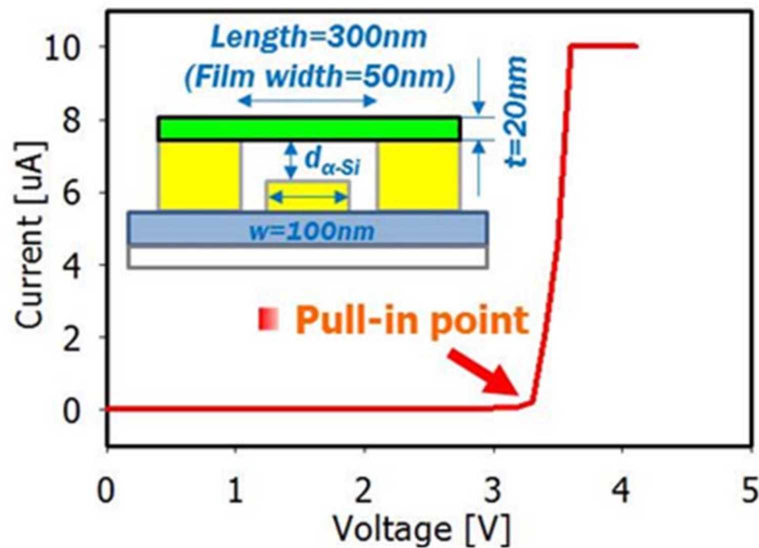


Figure 4.11: Current-Voltage Curve of a switch made of AC-SWNT beam.

Therefore, the on/off current ratio is more than 10^7, limited by measurement system capability, not by the device. In case of coarse SWNT bundles rather than membranes, there are multiple "Pull-in" events as shown in Figure 4.12. A possible cause of multiple pull-in events might be the existence of multiple unbound or poorly bound AC-SWNT threads. These multiple pull-in events were not seen in dense SWNT membrane devices.

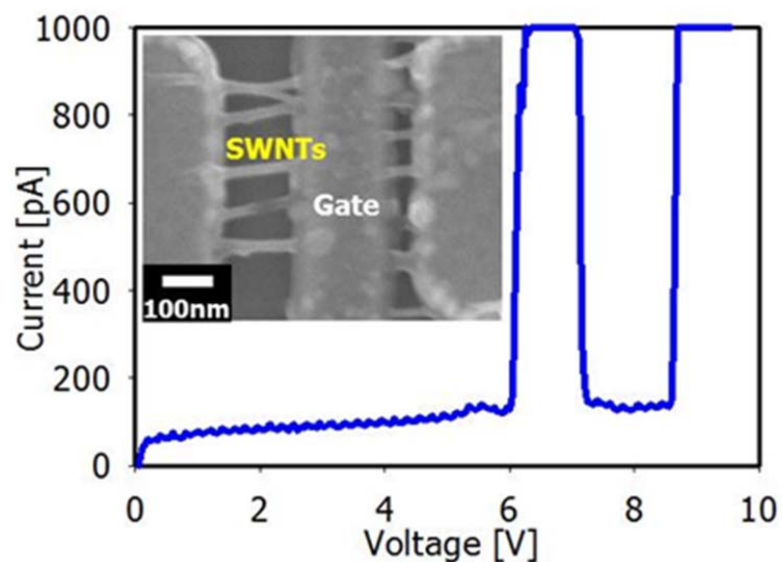


Figure 4.12: Schematic of pull-in voltage measurement set-up.

4.4.1.3. Beam Length Dependency

The pull-in voltages of all measured devices are in the range of 0.9~4.8 V depending on the beam length as shown in Figure 4.13. The measured data are much smaller than the calculated data using equation 2.20 and 2.21 as well as they have large variance, which will be discussed more in detail, in the section 4.4.1.4. This might be due

to the increased surface roughness of the gold contact and the existence of dangling SWNT bundles. It is well known that silicon has a high solid solubility in gold [276].

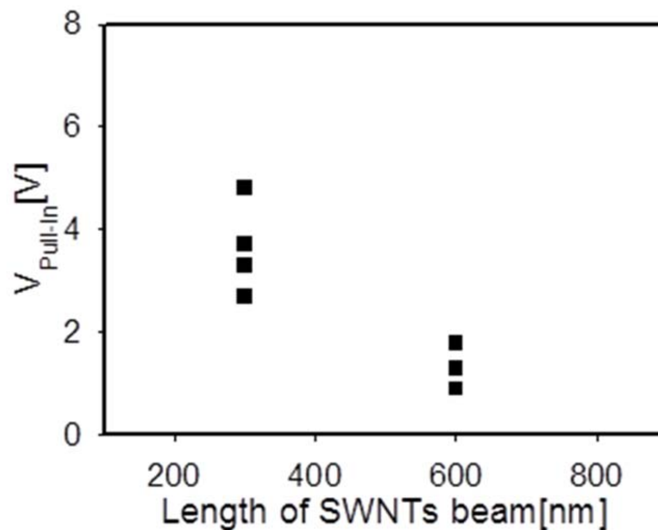


Figure 4.13: Pull-in voltage distribution depending on the length of SWNTs beam.

When gold is deposited in contact with amorphous silicon sacrificial layer, however, gold diffusion could be more enhanced compared to single crystal silicon due to presence of a high concentration of defects in the α-Si [276]. Figure 4.14 show the surface roughness of gold contact became worse after α-Si etching. When this happens, the effective air-gap would be decreased and the effective contact area would be increased due to this unwanted gold diffusion after removal of amorphous silicon. Moreover, the gold surface may be damaged during plasma etching of α-Si. The increased roughness of the gold contact may contribute to low pull-in voltage and its large variation, as will be discussed

in the next section.

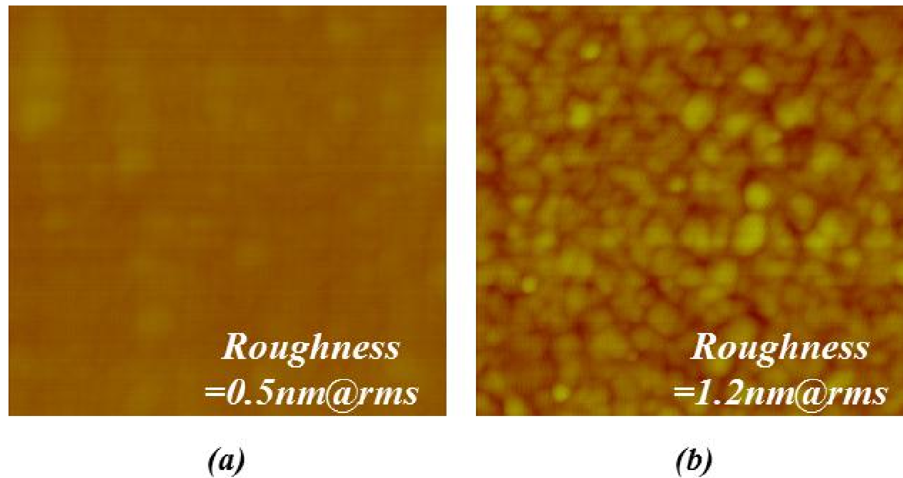


Figure 4.14: Gold Surface Roughness by AFM; (a) Before sacrificial α-Si deposition, (b) After Device Release by etching α-Si.

As shown in Figure 4.11, the switching event appears to be gradual done rather than the abrupt transition predicted for an ideal electromechanical switch. One possible reason is that dangling SWNT bundles or even discrete tubes may exist, which are not fused with the aligned-composite SWNT film. These structures would have a smaller air-gap than the SWNT film, which could result in contacting with gold electrode at a lower voltage. Moreover, the actual value of the air-gap would be stochastic. This would produce a large distribution of pull-in voltages at the same SWNT beam length.

4.4.1.4. Comparison with Pull-in voltage model

In this section, the pull-in voltage model is compared with the measured data from the fabricated 2-terminal switches. First, the closed-form pull-in voltage model for fixed-

fixed beam under concentrated load introduced in the section 2.3.2.1 is discussed. Then, the contact surface roughness effect on pull-in voltage will be discussed.

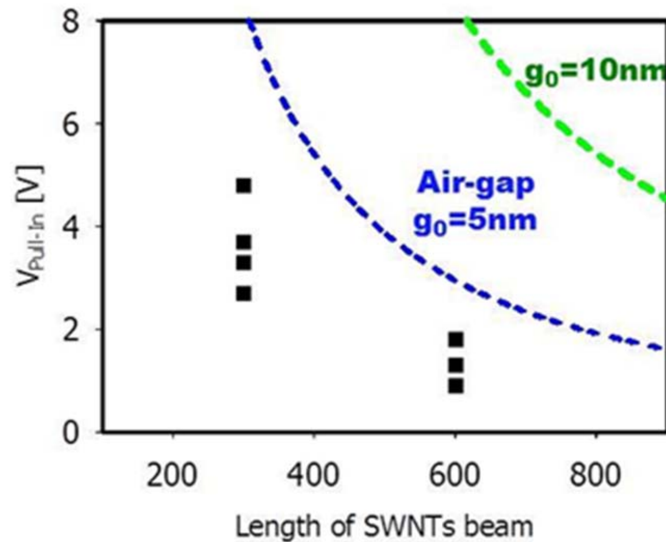


Figure 4.15: Comparison measured pull-in voltages with simple closed-form pull-in voltage model. (g_0 is the air-gap between free-standing beam and bottom electrode)

Using the two equations 2.38 and 2.39, the normalized pull-in voltage versus the hemisphere radius for various gaps could be predicted as shown in Figure 4.16. The influence of roughness to diminish the pull-in voltage becomes more significant for larger *R/d* values due to the increase in the capacitance and the associated electrostatic force [70]. Moreover, the dependency of pull-in voltage on surface roughness is increasing as fundamental air-gap is decreased. Moreover, recall that the gold contact surface roughness from AFM measurement was about 1.2nm. In case of assuming this value as the radius of the hemisphere in Figure 4.16, the pull-in voltage considering surface

roughness would become about 65% lowered for 5nm air-gap devices.

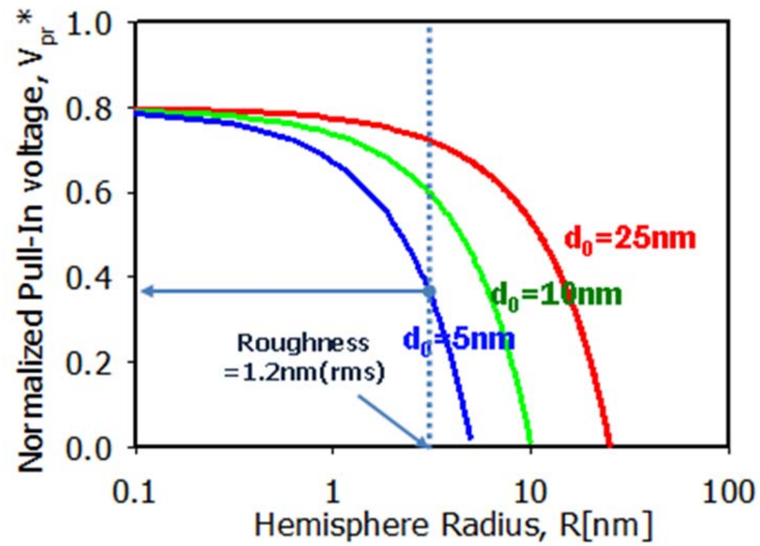


Figure 4.16: Kogut Model [70] for surface roughness effect on pull-in voltage.

Now the measured pull-in voltage is again compared with a new model considering the gold contact surface roughness based on Kogut study [70], as shown in Figure 4.17. The solid lines are from the revised pull-in voltage model which takes into account the effects of surface roughness. The dotted lines are the flat plate model. Now the dependence of the measured pull-in voltages with beam length can be explained. The narrowness of the gap required to fit the data may simply reflect and the presence of dangling SWNT bundles and/or beam sagging downward due to extrinsic biaxial compressive stress in the SWNT layer. Note that this does not mean that the effective air-gap would be 5nm, because this Kogut model considers only the bottom electrode surface

roughness effect. However, the aligned-composite SWNT film has also its own surface roughness and the surface roughness should be considered in a statistical view to simulate real contact surface roughness. It is likely that if one takes this into account, the actual gap would be closer to 10 nm. Finally we point out that the pull-in variation may be due to difference in the local film stress, delamination of individual bundles, or differences in electrode roughness.

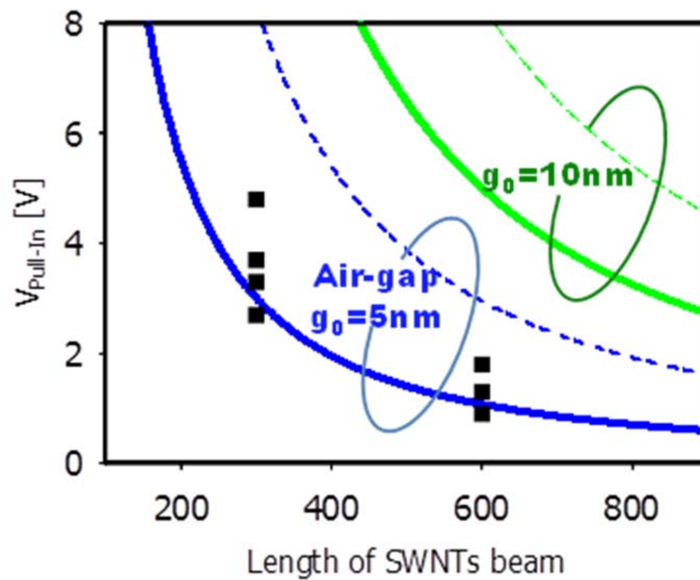


Figure 4.17: Comparison with measured pull-in voltage and Kogut Model [70] considering the contact surface roughness effect.

4.4.1.5. Hysteresis between Pull-In and Pull-Out Voltages

MEMS/NEMS devices may experience a large hysteresis between pull-in and pull-out voltages. The pull-out voltage is defined as the maximum voltage for the

MEMS/NEMS device to be switched off. This can be measured from a reverse voltage sweep. To measure this hysteresis, as shown in Figure 4.18 (a), the gate voltage is initially increased with forward direction up to pre-assigned maximum voltage then decreased to zero voltage. To ensure that the MEMS/NEMS device is actuated, the electrostatic force should be greater than the elastic restoring force on the movable beam. When the beam contacts the bottom electrode, two additional forces such as van der Waals force and short range forces are set up, which are negligible when the beam is far from bottom electrode and affected by contact surface roughness and species of interacting atoms [277].

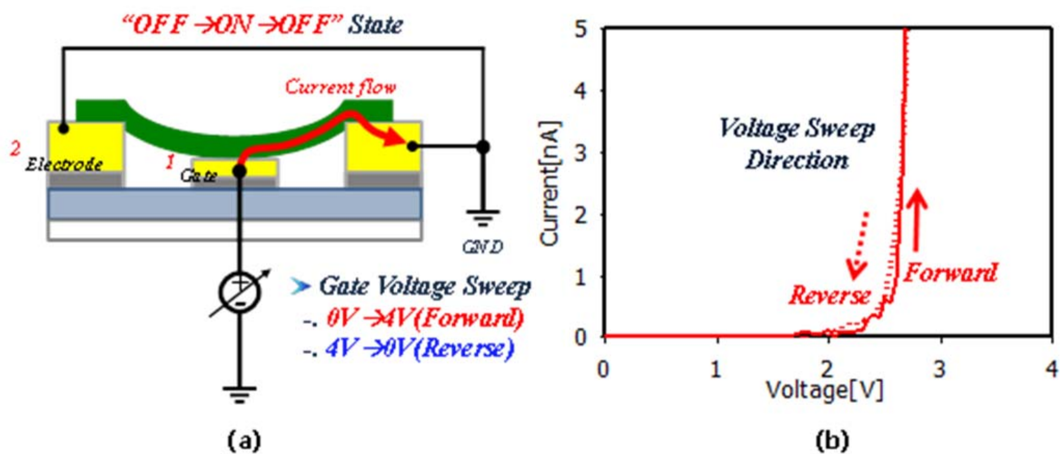


Figure 4.18: (a) Pull-in and Pull-out voltages measurement set-up, (b) Measured I-V characteristic of AC-SWNT Beam NEMS Switch.

Therefore, the elastic restoring force on the beam should be larger than those two forces for the MEMS/NEMS devices to be successfully turned off.

From the hysteresis measurement of our fabricated 2-terminal NEMS switch, as shown in Figure 4.18 (b), we found very small difference between pull-in and pull-out voltages, typically 20 to 100 mV This small hysteresis suggests that our devices have very small stiction forces. Certainly the formation of textured electrodes on both top and bottom of the switch contribute to this effect. It may also be the case that CNTs, due to their low chemical reactivity, have inherently low stiction effects.

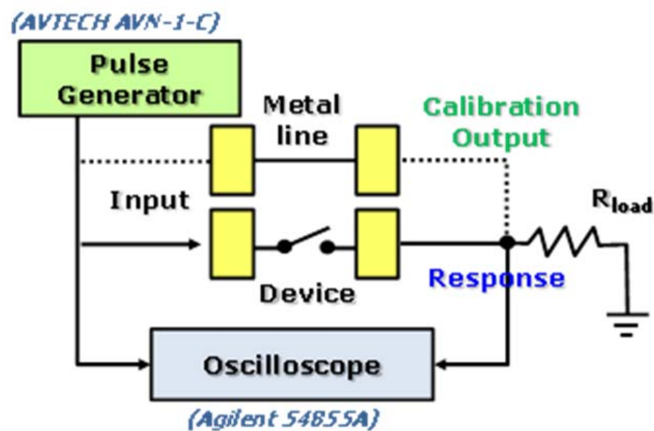
4.4.2. Switching Delay

4.4.2.1. Measurement set-up and measured switching delay

The switching delay of fabricated 2-terminal switch using aligned-composite SWNT thin film was measured. Figure 4.19 (a) and (b) show the switching delay measurement procedure, consisting of a pulse generator (AVTECH AVN-1-C) providing step pulses with 200 psec rise time and a high speed digital oscilloscope (Agilent 54855A). This measurement scheme was originally demonstrated by Kaul, *et al* [32]. To remove the time delay associated with the probe stand and wires, the "Calibration Output (an actual input for the device)" was compared to "Device Output". The "Calibration Output" was measured by shorting the probes together on a metal strip on chip without the switch device. This result measures the parasitic delay by the test instruments and metal pads themselves, such as that arising from cable lengths, stray capacitances, and inductances both on- and off-chip.

Figure 4.20 shows the test result of switching characteristics on the device. The best

output signal was 600psec delayed to the calibration output [278]. Ringing noises in the calibration and device output likely arise from the uncontrolled impedance lines and the impedance mismatch between the AC-SWNT switch and the test instruments. In the next section, the measured switching speed is compared with the theoretical model.



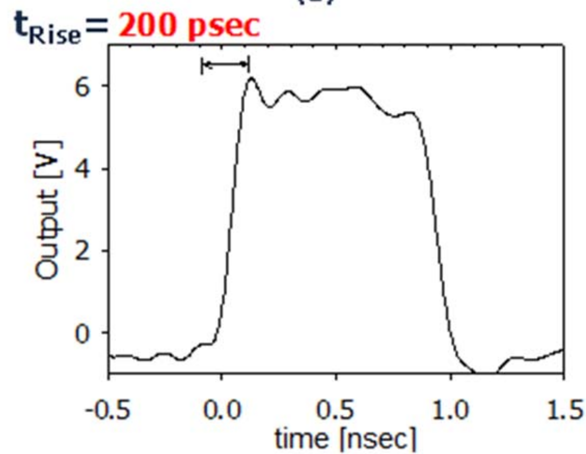


Figure 4.19: (a) The switching delay measurement setting, (b) High speed pulse generator output pulse with 200psec of rising time.

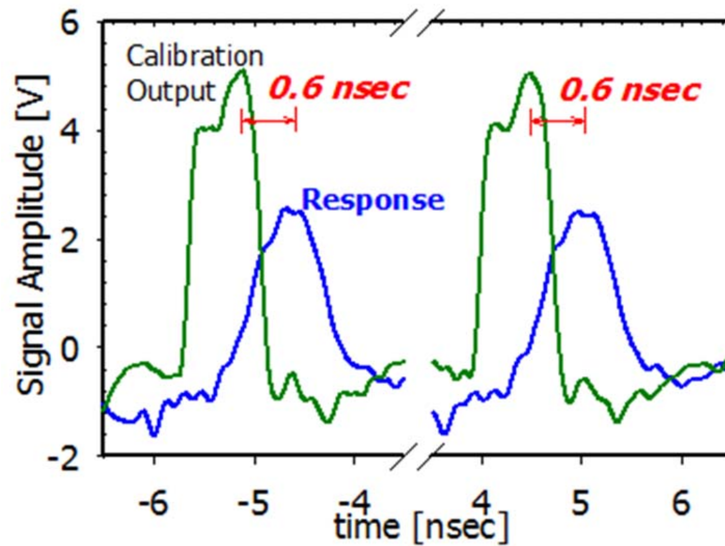


Figure 4.20: Test result of switching delay on our device by comparing with the calibration output (=input).

4.4.2.2. Comparison with theoretical model

Using two equations 2.53 and 2.58 in the Chapter 2, the switching speed was calculated and compared with the measured data in Figure 4.21. In the graph, the blue, green, and red lines represent the cases of 100GPa, 350GPa, and 850Pa of Young's modulus, respectively. For model calculation, the pull-in voltage (V_p) and supply voltage (V_s) was 3V and 5V from measurement, respectively. The mass density of the film was assumed as 1g/cm^3. And the applied film thickness was 20nm from the AFM measurement [63].

The measured switching speed is about 600psec equivalent to 1.6GHz at 300nm of beam length. However, this is about an order smaller than the switching speed model (Section 2.3.4). This difference may be due to the assumptions used to obtain the

switching speed model and the fundamental resonant frequency as well as to measure Young's modulus. For model extraction, we assumed that the free-standing beam is uniform and slender, also that it is composed of a linear, homogeneous, isotropic elastic material without axial loads and any rotary inertia and shear deformation can be neglected [64]. However, the aligned-composite film does not satisfy these assumptions. Moreover, we measured the Young's modulus of the aligned-composite film from an AFM measurement assuming the residual stress of the beam is negligible. As introduced, we used α-Si as a sacrificial layer, which is highly compressive material. Thus, the released beam has an extrinsic biaxial tensile stress after α-Si removal. It is likely that the real Young's modulus is smaller than our measured value.

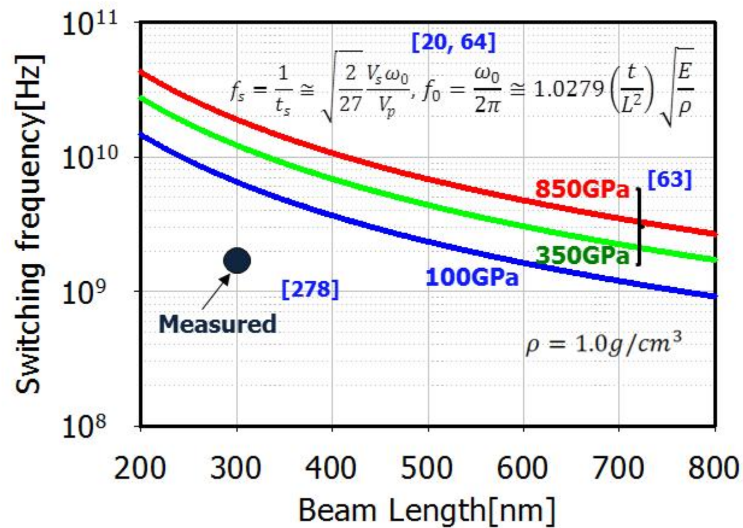


Figure 4.21: Comparison with 1st mode of fixed-fixed beam resonance frequency.

4.4.2.3. Comparison with Literatures

The switching delay and pull-in voltage of our AC-SWNT beam switches are significantly less than other published MEMS devices [49] as shown in Figure 4.22. Major reasons might include the very low mass density of the carbon nanotube composite films, the high spring constant [279], and the low pull-in voltage. Only Kaul *et al* [32] at Caltech reported a 2.8nsec switching time, equivalent to about 360MHz, at 2V of pull-in voltage using a SWNT bundle bridge, which was grown through CVD. This CNT growth method is reproducible random process; positioning of individual CNTs or CNT bundles is notoriously difficult.. The process described here is based on continuous film formation followed by conventional lithography and etching. It is therefore, much more reproducible.

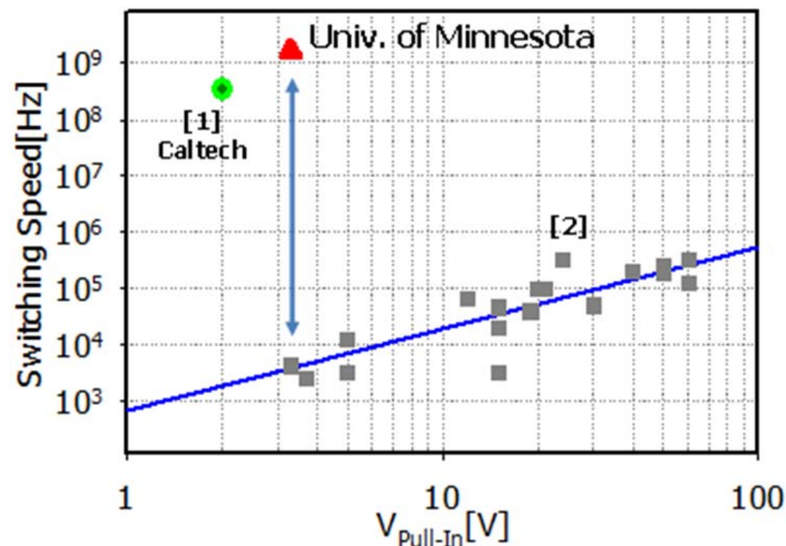


Figure 4.22: Comparison with other literature reports- the line indicates a slope of unity.

4.5. Issues

4.5.1. Reliability

Despite the exceptionally excellent characteristics, the aligned-composite SWNT film has a critical reliability issue. Devices are quickly burned out by Joule-heating due to the copolymers, which are highly resistive and low transition temperature. The longest lasting devices survive maximum current flow for only a few minutes. However, most devices were failed very quickly. There are three possible causes: high film resistivity, the low melting point of PDDA, and high contact resistance between the gold contacts and the beam.

The measured film resistivity is about 8.7×10^{-3} $\Omega\cdot$cm [63], which is a thousand times higher than other popular materials for MEMS application such as gold (2.44×10^{-6} $\Omega\cdot$cm) [280], aluminum (2.82×10^{-6} $\Omega\cdot$cm) [281], titanium nitride (3.0×10^{-6} $\Omega\cdot$cm) [282] and tungsten (5.60×10^{-6} $\Omega\cdot$cm) [281]. Therefore, the Joule heating is at least thousand times higher for the same current density.

Second, the PDDA used for a copolymer is composed of carbon, hydrogen, nitrogen, and chloride with the C:H:N:Cl ratio 8:12:1:1. At temperature above 130˚C, the hydrogen and nitrogen components of PDDA are able to react with oxygen and produce H_2O and N_xO_y, respectively. In the worst case, it is possible to be fully combust PDDA under these conditions [266].

Third, most metals make a schottky contact with carbon nanotubes. Especially, the bottom of the aligned-composite SWNT film is comprised of stacks of copolymers, which is highly resistive. As a result, its contact resistance is very high.

Therefore, due to these three factors, our devices with the aligned-composite SWNT thin film could not operate for longer than a few minutes. Microscope inspection on tested devices indicate a color change of the center of device when the device was failed, which means the SWNT film and gold contact were electrically connected.

4.5.2. Throughput

The film preparation of aligned-composite SWNT film is based on dielectrophoresis, which is well controllable with a simple control circuit and quick. For a 20nm thick film, it only takes a few minutes. However, this process is required to have two electrodes to apply an ac electric field. It is not easy to extend this approach to fabricate complex circuits and for wafer-level applications.

4.6. Conclusions

Functional sub-nanosecond fixed- beam switches have been developed using well-aligned self-assembled single-walled carbon nanotube (SWNT) composite membranes, which were prepared by dielectrophoretic self-assembly process with Layer-by-Layer self-assembly. The dense membranes were successfully patterned to form submicron beams by E-beam lithography and oxygen plasma etching. Fixed-beam switches using these membranes successfully operated with approximately 600 psec switching delay and as low as 3 V dc pull-in. From this experiment, we confirmed that the SWNT based thin film have the potential to make fast MEMS switches with a low operation voltage due to

its low mass density and high stiffness.

However, the aligned-composite SWNT film uses copolymer stacks, which result in early device failure. Moreover, the dielectrophoretic deposition process is not applicable for complicated circuits and wafer-level applications because the two electrodes must be actively powered during the film deposition process for each device. Therefore, a new SWNT deposition process is necessary to resolve these problems and still use the unique physical and electrical properties of SWNT.

CHAPTER 5. FABRICATION OF PURE SWNT THIN FILM BASED 3-TERMINAL MEMS SWITCH

5.1. Overview

In the previous work, we demonstrated functional 1.6GHz 2-terminal NEMS switches using the aligned-composite SWNT membranes [63, 278]. The DC pull-in voltages of the switches ranged from 0.9V to 4.8V, depending on their sizes. These values are quite low for high speed switches [278]. To prepare the actuator beam material in this work, we used the layer-by-layer (LbL) self-assembly of SWNTs by dielectrophoresis [63]. However, this aligned composite SWNT membrane switch has two critical drawbacks.

First, the dielectrophoretic deposition process is not easy to extend to a wafer level deposition process. The current process would be inadequate for a complicated circuit demonstration because it requires two electrodes for every single device. This results in the increased layout complexity and drastically decreased area efficiency.

Second, the copolymer used as a positive charged layer for layer-by-layer process, poly(diallyldimethylammonium chloride) (PDDA), is electrically insulating. The presence of the insulating copolymer results in a high resistivity unless the CNTs are aligned. Moreover, the switch is naturally exposed to high temperature condition by joule heating during a switching operation, but the PDDA has a low melting temperature. This results in poor reliability of high speed switching devices.

To resolve these issues, it is critical to develop an LbL self-assembly process to

produce purely carbon nanotube based thin film without the use of copolymers. In this work, we discuss a copolymer-free SWNT film deposition process based on the LbL self-assembly and its electrical properties. Moreover, we demonstrate a 3-terminal MEMS/NEMS switch successfully built using this all SWNT thin film as a digital logic element.

5.2. Pure SWNT Thin Film Preparation

As reviewed in the Chapters 3 and 4, the LbL assembly is a simple and adaptable process [227, 294-296]. However, our previous aligned composite-SWNT thin films have revealed reliability problem and is not applicable to wafer level and complicate circuits as discussed in the chapter 4. To resolve this issue caused by the polymer components, LBL films have been made entirely from carbon nanotubes. Lee *et al* made a pure multi-walled nanotube (MWNT) film [286]. CNTs have been modified to have negative carboxylic acid functional groups [288, 298] and positive amine functional groups [299-300] on their exterior. In our work, we have taken the same approach of making an all CNT film, but we have elected to use single-walled nanotubes (SWNT), due to their better electrical properties, relative to MWNTs [301-302]. Additionally, we introduced two different approaches to functionalizing the SWNTs, which will be introduced in the next two sections. It is important to note that all of the work described in Section 5.2.1 including functionalizing SWNTs and preparing SWNTs dispersions were conducted by Professor Taton’s group (Chemistry Dept.). It is presented here since these solutions were

used to deposit the CNT films, which were then used to fabricate devices.

5.2.1. Functionalization of SWNT

5.2.1.1. Negatively Charged SWNT Dispersion

In the first approach, SWNTs are treated with sulfuric and nitric acids to form carboxylic acid functional groups, which can then be used as negative SWNTs. This sulfuric and nitric acids treatment is simply to oxidize the exterior of carbon nanotubes [288]. Pristine SWNTs were purchased from Cheaptubes.com (>90% purity, 5-30 μm length, 1-2 nm outside diameter). SWNTs were refluxed in concentrated H_2SO_4/HNO_3 (3/1 v/v, 96% and 70%, respectively) for 1.5 h to give carboxylic acid functionalized SWNTs (SWNT-COOH). The reaction mixture was then diluted with deionized Milli-Q water (14 MΩ· cm) to pH > 2, and then was filtered on a nylon membrane filter (0.45 μm)

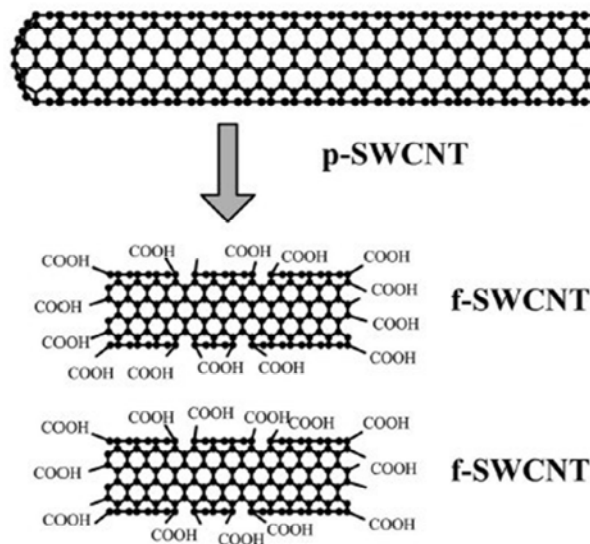


Figure 5.1: A schematic process of chemical functionalization of pristine SWCNT by concentrated acid treatment; Reproduced from [155].

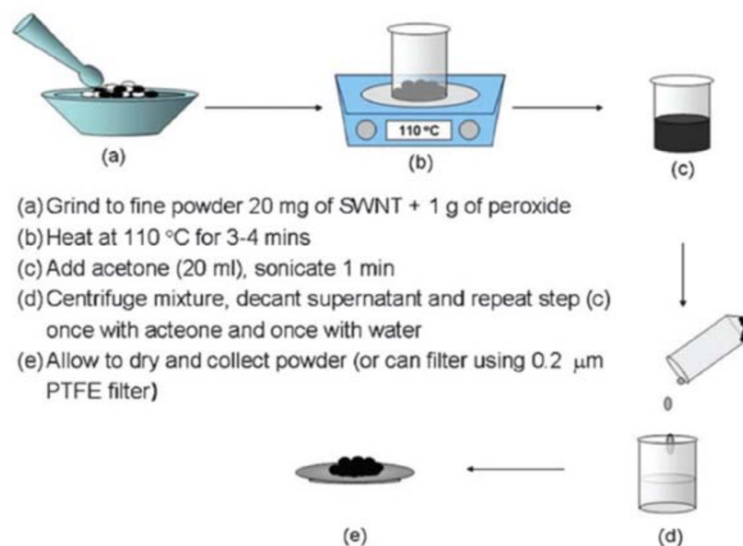


Figure 5.2: A schematic process of chemical functionalization of pristine SWCNT by Succinic Acid Peroxide (SAP) method; Reproduced from [303].

[155, 286-288]. The SWNT-COOHs were rinsed with deionized water several times as described in Figure 5.1.

In the second approach, the SWNTs are treated with succinic acid peroxide (SAP) to introduce carboxylic acid functional groups [303]. This approach uses radical intermediates to introduce carboxyethyl units specifically to the double bonds on the SWNT sidewalls. It is thought that this type of treatment does not damage the SWNTs and shorten them to the extent that nitric acid oxidation does [287], better preserving the desired SWNT structure. Figure 5.2 shows the procedure for the reaction. SWNT and succinic acyl peroxide are ground to a fine powder. This powder is heated in a small beaker at 100 to 110 ˚C for 3 to 4 min. Upon cooling the melt, acetone is added and the mixture is sonicated to disperse the SWNT and dissolve the excess molecules. After centrifuging, the supernatant is decanted. This last step is repeated once more with

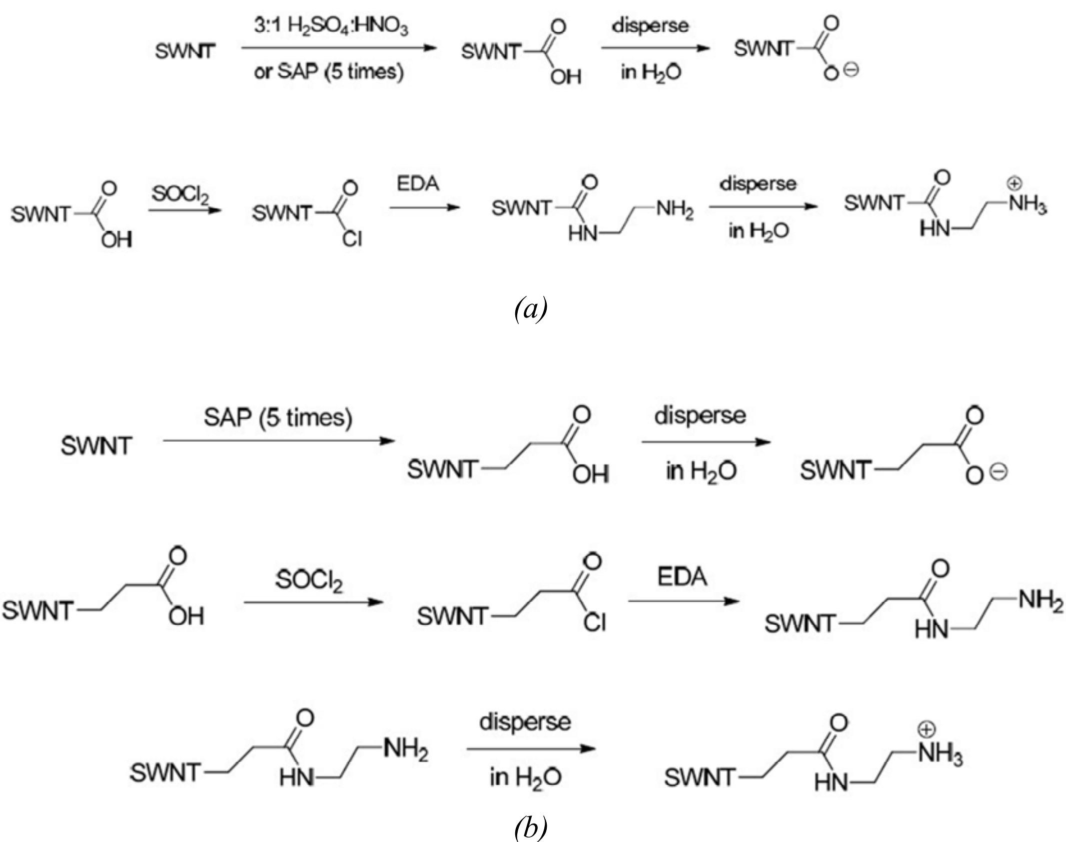


Table 5.3: Functionalization of SWNTs (a) via nitric acid oxidation pathway, and (b) (b) via succinic acid peroxide oxidation pathway. [Courtesy of Prof. Taton group at Chemistry Department].

acetone and then water. After purification, the final solid can be left to dry and then collected. To increase the number of functional groups on the SWNT sidewalls, the reaction procedure was repeated for 5 times.

5.2.1.2. Positively Charged SWNT Dispersion

The amine group was attached to the exterior of negatively functionalized SWNTs using two approaches, as shown in Figure 5.3. The first step was chlorination by

refluxing in $SOCl_2$ (Sigma-Aldrich) for 12 hours. The excess $SOCl_2$ was removed by evaporation, and then the chlorinated SWNTs were treated with ethylene diamine (EDA, Sigma-Aldrich) in refluxing, dry toluene for 24 hours [286]. Then it was filtered and rinsed with deionized water on a nylon membrane filter with 0.45μm pores.

5.2.1.3. Evaluation of Functionalized SWNT dispersions

The stability and relative charge of the SWNT functionality were analyzed by zeta potential analysis using a Malvern Zetasizer instrument by Prof. Taton group. All measurements were made using 1.0 mg/mL dispersions. Each measurement is the average value of three sets of 100 measurements taken. Typical results for each type of material are presented in table 5.1.

The magnitude of the zeta potential of materials synthesized via the SAP oxidation pathway is larger relative to the materials synthesized via the nitric acid oxidation pathway. This suggests that the SAP oxidation pathway may functionalize the SWNTs to a greater extent. Also, for functionalized SWNTs dispersions the zeta potential depends on the pH of the dispersion [286]. The carboxylic acid group needs to be deprotonated to have a negative charge. Because of this, as the pH increases, the zeta potential becomes more negative. Conversely, the SWNTs that have amine functionality become protonated as the pH is lowered, giving a positive charge. This causes the zeta potential of the positive dispersions to become more positive as the pH is decreased.

Oxidation Method	Charge	pH	Zeta Potential (mV)
Nitric Acid	Positive	4.5	-36.4
Nitric Acid	Negative	2.5	37.9
Succinic Acid Peroxide	Positive	4.4	-55.6
Succinic Acid Peroxide	Negative	2.6	45.9

Table 5.1: Representative Zeta Potential Values for Charged SWNT Dispersions [Courtesy of Prof. Taton group at Chemistry Department].

Sufficiently functionalized dispersions have been stable for more than 3 months. Figure 5.4 shows the SWNTs in each dispersion are fully precipitated due to the attractive electrostatic force, when the two oppositely charged SWNT dispersions are just mixed together.

Figure 5.4: Precipitating reaction occurred by mixing two oppositely charged SWNT dispersions.

5.2.2. Detailed Deposition Process

In general, the LbL self-assembly deposition is done by simple dipping process in the two oppositely charged dispersions repeatedly and alternatively in turn, as shown in Figure 5.5. The substrate was treated with O_2 plasma using STS etcher at 100 W, 100

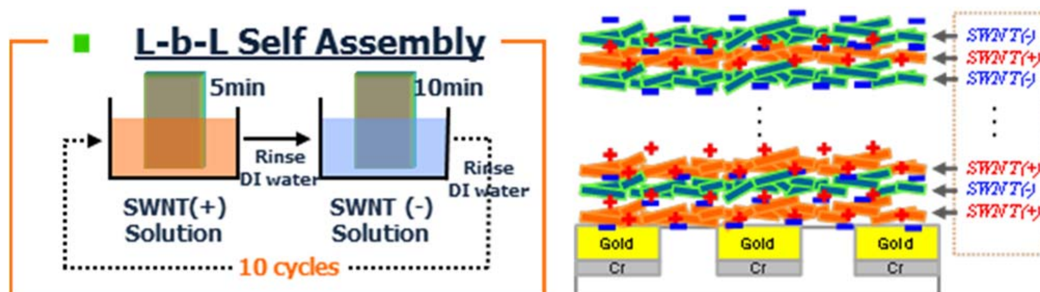


Figure 5.5: Schematic of copolymer-free SWNT film deposition based on layer-by-layer Self-assembly.

mTorr, and 100 sccm oxygen flow for 5 minutes so that its surface would be hydrophilic. Then, the substrate was dipped into the positively functionalized SWNT dispersion for 5 minutes. To remove unreacted SWNT debris, it was rinsed with Milli-Q water for 2 minutes and again for 1 minute. This rinse step is quite important because an insufficient rinse might ruin the next SWNT dispersion, which means that most of SWNT particles and bundles would precipitate out of solution. After rinsing, the substrate was dipped into negatively functionalized SWNT dispersion for 10 minutes and it was rinsed with Milli-Q water for 2 minutes and 1 minute once again. This cycle of dipping and rinsing was repeated until the desired SWNT film thickness was achieved. The dipping time for each dispersion was determined by quartz crystal microbalance measurement using QCM200,

Stanford Research Systems. A QCM measures a mass per unit area by measuring the change in frequency of a quartz crystal resonator. The resonance is shifted by the addition or removal of a small mass due to oxide growth/decay or film deposition at the surface of the acoustic resonator. The QCM can be used under vacuum, in the gas phase ("gas sensor", first use described by King [304]) and more recently in liquid environments [305-306]. It is useful for monitoring the rate of deposition in the LBL self-assembly. Figure 5.6 shows the frequency shift depending on the number of dipping cycles in the LBL self-assembly for all-SWNT thin film deposition. The red squares correspond to the frequency shift (from the initial value) after the sample wafer was dipped into the positively functionalized dispersion. Each blue square represents the frequency shift after the sample wafer was dipped into the negatively functionalized dispersion. The average frequency shift is about 92.2Hz for a dipping into the positively functionalized SWNT

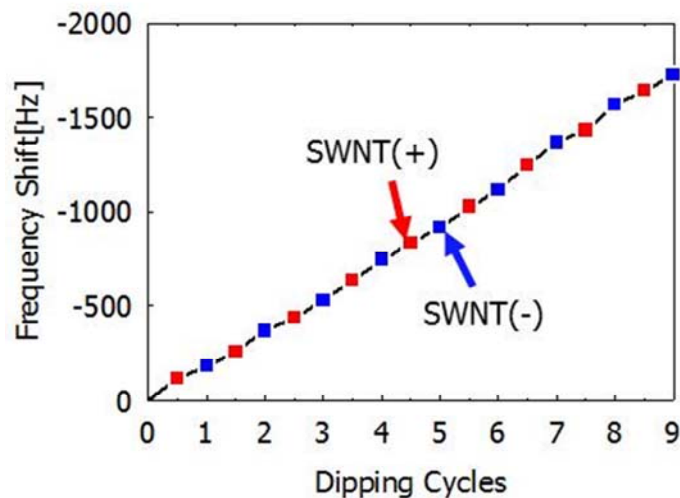


Figure 5.6: Frequency shift measurement of quartz crystal microbalance test for all-SWNT thin film deposition using LBL self-assembly process.

dispersion for 5 minutes and 99.1Hz for dipping into a negatively functionalized SWNT dispersion for 10 minutes. In Figure 5.5, the total frequency shift is linearly proportional to the number of dipping cycles. This signifies that the film thickness is linearly proportional to total dipping cycles, indicating that this process is controllable and predictable.

Figure 5.7 shows the optical microscope and SEM (JEOL6700) images for various numbers of dipping cycles. From the optical microscope images, the film color becomes darker with increasing number of dipping cycles, which means that the film thickness is increasing. The SEM images support this interpretation.

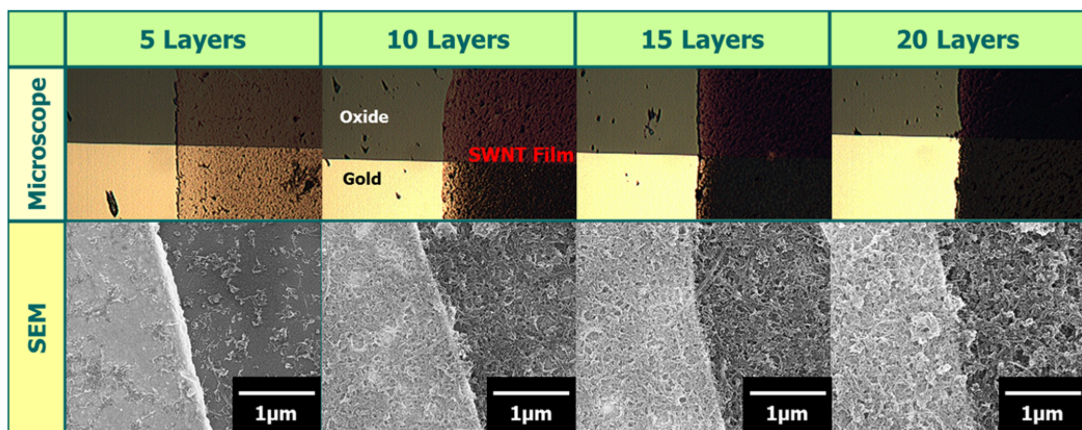


Figure 5.7: Optical microscope and SEM images as the dipping cycles are increased.

Figure 5.8 shows the deposition rate per each bi-layer dipping and rinsing cycle and the uniformity of deposited film thickness across a 4-inch wafer after a 10-cycle deposition. The calculated deposition rate is about 10nm per bi-layer deposition cycle. Moreover, on the 4-inch wafer, the SWNT film was uniformly deposited, with a standard

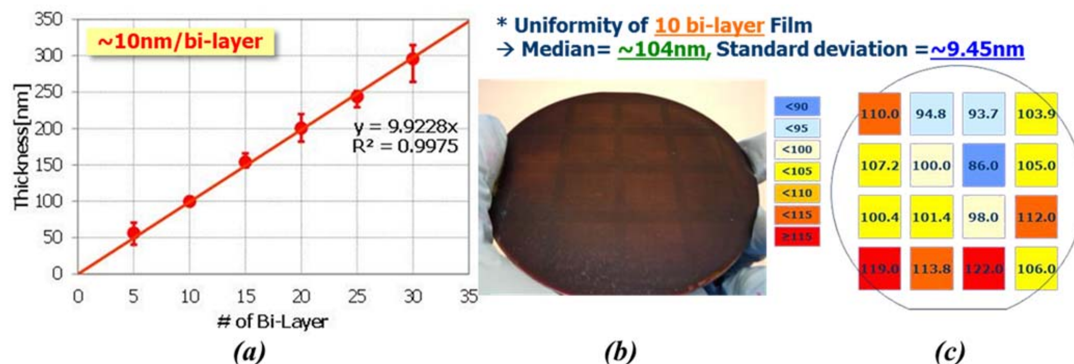


Figure 5.8: (a) Deposition rate per each bi-layer, (b) As-deposited 4-inch wafer, (c) Within wafer uniformity of all-SWNT thin film thickness after 10 bi-layer deposition.

deviation was less than 10% of median thickness despite the rudimentary deposition process. No attempt was made to improve this uniformity.

5.2.3. Film Characterization

In this section, the structural, mechanical and electrical properties of a pure SWNT thin film deposited by LbL process are discussed.

5.2.3.1. Structural Observations

In the all-SWNT films deposited by LbL self-assembly, the SWNTs are randomly distributed and the film thickness is proportional to the number of dipping cycles. SEM and AFM were used to measure the topology of all-SWNT film surface as shown in Figure 5.9. Each SWNT bundle in the films is randomly distributed. The root-mean-square surface roughness of the film increased at the rate of 1.3 nm per cycle.

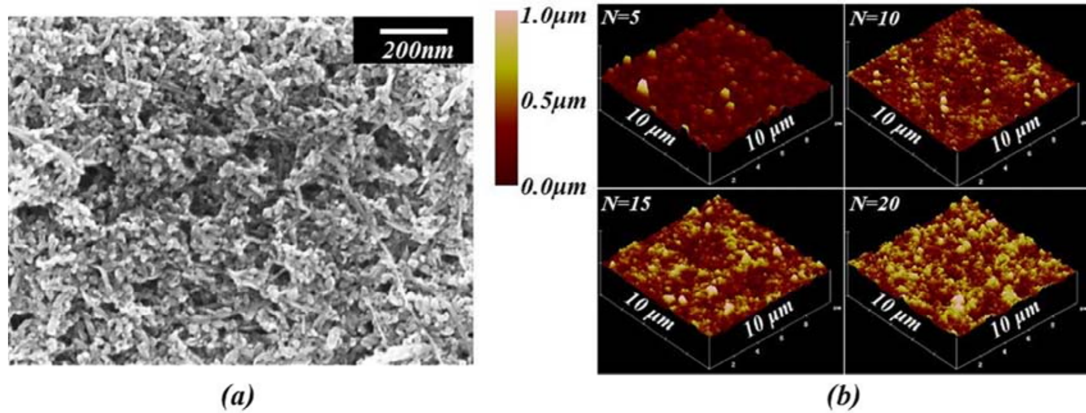


Figure 5.9: (a) A SEM image on the sample with 10-cycle deposition, (4) AFM images depending on the numbers of dipping cycles.

5.2.3.2. Mechanical Properties

The Young's modulus of the all-SWNT thin film was measured bynanoindentation tests with Hysitron's Triboindentation system by Professor Cui's group. Nanoindentation is a popular method for determining the mechanical properties of thin films due to its ability to control indentation depth on the nanoscale. It is a common method for measuring the elastic modulus and hardness of small volumes of material due to its ease of use. There are minimal sample preparation requirements, specimens can be tested several times, and different volumes of material can be examined through the appropriate choice of loading conditions and tip geometries [307].

Nanoindentation has been possible through the development of instruments that are able to continuously measure the force and displacement during indentation. In addition, the resolution of measured force and displacement of nanoindenation systems is of order nanonewtons and nanometers, respectively. Figure 5.10 is a schematic of the transducer assembly in Hysitron's Triboindentation system [308]. The transducer consists of three parallel capacitor plates; the top and bottom plate are held fixed, while the middle plate,

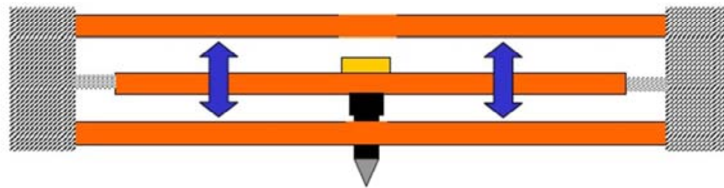


Figure 5.10: Transducer assembly in Hysitron's triboindentation system; Reproduced from [308].

to which the probe is connected, is held by leaf springs and is allowed to move in the vertical directions. By manipulating the voltages on each capacitor plates, the position of the tip can be precisely controlled [308].

From this triboindentation test, the spring constant of samples can be easily extracted by the ratio of applied force (F) and the deflection (δ). Moreover, as the deflection increases, the linearity of the deflection-applied force curve might disappear due to the transition to plastic mode or penetration of indent tip into beam. So the yield strength can be found at the point where linearity in force-deflection curve disappears.

The first step for extracting mechanical properties of all-SWNT film was to make free-standing beams as shown in Figure 5.11. The fabricated devices have a 310nm thick all-SWNT film and a 500nm high air-gap. The beam length was about 12.2µm and the device width was 4.7 µm, as measured from the SEM images.

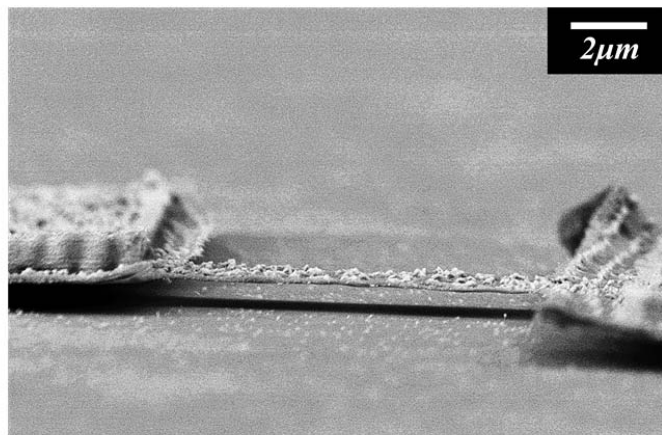


Figure 5.11: A SEM image of free-standing all-SWNT thin film for triboindentation test.

The Young's modulus of the all-SWNT thin film was initially extracted from the relationship between the spring constant and the modulus through the triboindentation tests on the fabricated devices. In the fixed-fixed beam structure, when a loading (F) is applied at the center of free-standing beam, it would be deflected (δ) [20], as shown in Figure 5.12.

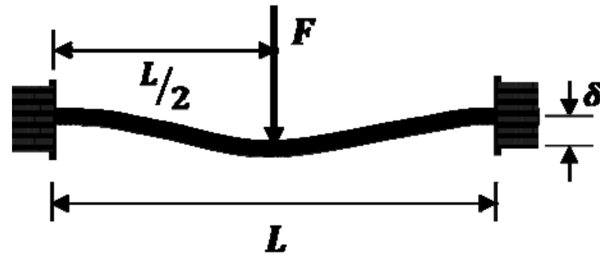


Figure 5.12: Fixed-Fixed beam deflection due to a loading at the center; Reproduced from [20].

The deflection of fixed-fixed beam due to a loading (F) at the center of beam is given by

$$\delta = \frac{FL^3}{192EI}, \tag{5.1}$$

where the L, E, and I are the length, Young's modulus and bending moment, respectively [20]. The bending moment for rectangular cross-section is given by

$$I = \frac{wt^3}{12}, \tag{5.2}$$

where the "*w*" and "*t*" are the width and thickness of the beam. Using Equation 4.2, the equation 4.1 can be rewritten as

$$\delta = \frac{FL^3}{16Ewt^3}. \tag{5.3}$$

By rearranging the Equation 4.3, the Young's modulus can be obtained by

$$E = \frac{L^3}{16Ewt^3}\left(\frac{F}{\delta}\right) = \frac{kL^3}{16Ewt^3}, \tag{5.4}$$

where k is the spring constant of fixed-fixed beam.

From Equation 5.4 and the triboindentation tests, the Young's modulus and yield strength were extracted as summarized in the Table 5.2. The tested samples underwent three different thermal treatments to improve the film resistivity, which were "Untreated", "Annealed at 150˚C for 2hours at 2~5mT" and "Annealed both at 150˚C for 12hours at 2~5mT and at 300˚C for 2hours at H_2/N_2 ambient". The extracted Young's modulus ranged from 500GPa to 900GPa and the yield strength was ranged from 1500MPa to 2000MPa. This result is much higher than the popular material for MEMS/NEMS applications such as aluminum (E=69GPa, Y=10MPa) [309] and gold (E=80GPa, Y=120MPa) [310]. The samples annealed at 150˚C for 2hours at 2~5mT showed a slightly smaller median value of Young's modulus compared to other samples, however, the difference is within the measurement error of the instrument. This implies that the thermal treatment on the all-SWNT film does not measurably change its mechanical properties. This is surprising as the failure of the film was anticipated to occur at CNT/CNT interfaces which would be affected by the thermal cycle.

Parameter	**Young's modulus E (GPa)**		**Yield Strength Y(MPa)**	
	Median	**σ**	**Median**	**σ**
Untreated	**624**	**132**	**1784**	**171**
Anneal_150˚C/12hrs	**554**	**129**	**1742**	**310**
150°C/12hrs@Vacuum & 300°C/2hrs@H_2/N_2	**704**	**145**	**1729**	**263**

Table 5.2: Extracted Young's modulus and yield strength from triboindentation tests (Courtesy of Prof. Cui group at Mechanical engineering department).

5.2.3.3. Electrical Properties

Film Resistivity

The electrical properties of 110 nm thick all-SWNT films were characterized as shown in Figure 5.13. The width of the measured SWNT film bar resistors is 100 μm and their lengths are 700, 1000, 2200, and 4200 μm, respectively.

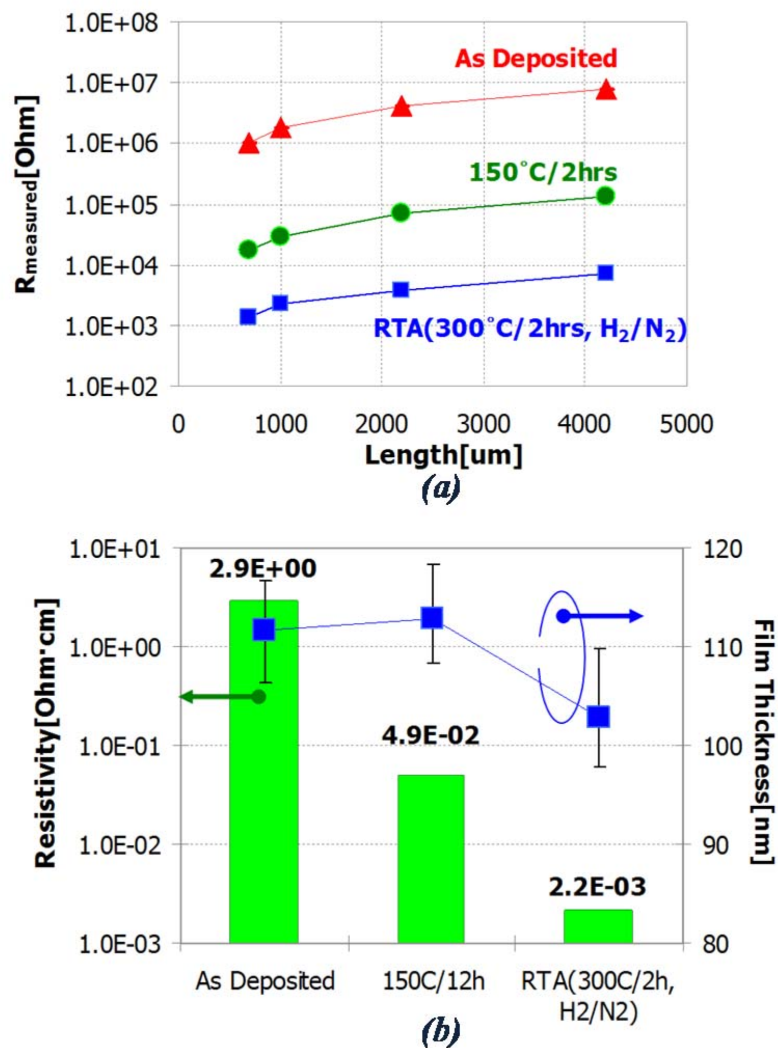


Figure 5.13: (a) Measured resistance of 100um wide bar resistor versus its length and (b) Extracted film resistivity and film thickness depending on thermal treatment.

The resistance was measured at 1.0 volt and the resistivity was estimated using the slope of the resistance versus length plot. The extracted resistivity was $2.9\Omega \cdot cm$, as shown in Figure 5.13(b), which is larger than literature values which are typically order of $10^{-3}\Omega \cdot cm$ [266, 273, 311-312]. This may result from the disruption of the conjugated carbon sp^2 orbitals on the SWNT exterior surface with the formation of surface functional groups.

To improve the resistivity of the film, thermal treatments were applied. As with the MWNT films of Lee *et al* [286], this was very effective in reducing the film resistivity. The first step is to anneal the film at 150˚C for 12 hours in vacuum (2 to 5mTorr) to form an amide between the –COOH and –amine functional groups. The film resistivity decreased about two orders of magnitude to $4.92\times10^{-2}\Omega \cdot cm$ after this anneal. This could be attributed to improved electron flow between adjacent SWNTs that are cross-linked via amide formation [286]. The second anneal was performed at 300˚C in a hydrogen atmosphere for 2 hours to remove the residual surface functional groups on the SWNTs [286]. The film resistivity after this anneal was $2.19\times10^{-3}\Omega \cdot cm$. This is about four times smaller than that of our previous aligned composite film deposited through copolymer based LbL process [63]. The film thickness after this second anneal was reduced by about 10% from the original value. We believe this is due to shortened average contact distance between coarsely connected SWNT bundles, in turn, which results in a further decrease of the film resistivity.

Specific Contact Resistance

The specific contact resistance could be estimated by fitting the measured resistances of contact chains [313], as shown in Figure 5.14. All bar resistors have two contacts, whose length and width are all 100um. The contact chain test structure has 50 SWNT film islands that are 4um wide and 30um long. For each island, there are two gold contacts. Therefore, there are 100 contacts with dimensions 4um long and 10um width. The extracted specific contact resistance was $6.3 \times 10^{-9} \Omega \cdot m^2$ from the contact chain measurement method in case of fully annealed films. This is comparable with other reports [313-315]. Moreover, the contact resistance could be further improved as well as reduced by adopting other metals as electrodes such as platinum or palladium [314, 316].

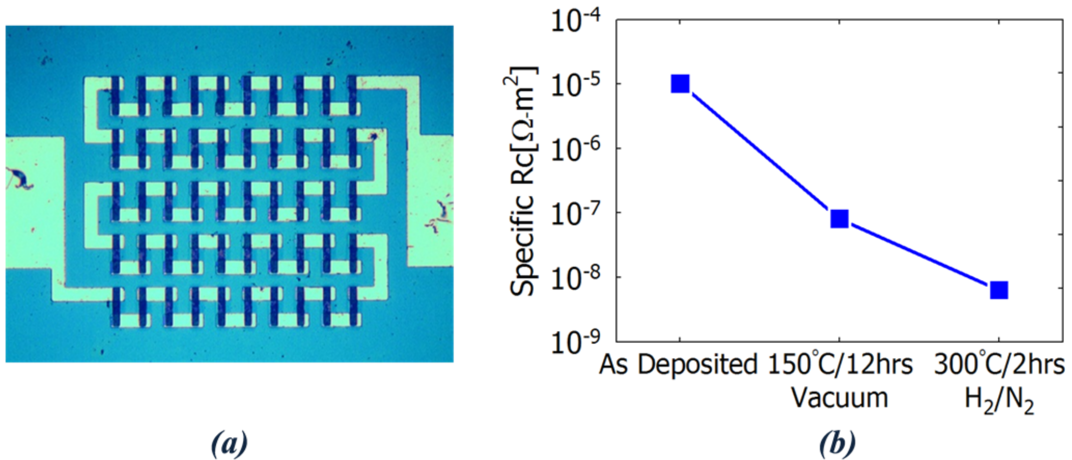


Figure 5.14: (a) Test structure of contact chain, (d) Estimated specific contact resistance.

5.3. Three-Terminal Device Fabrication

5.3.1. Initial Attempts & Issues

We fabricated three terminal MEMS switches for digital logic applications. In our initial attempts, substrates with 70 nm Au / 10 nm Cr electrodes were prepared with a conventional lift-off process. However, this produced high metal fences at the edge of photoresist, as shown in Figure 5.15. Since the cantilever film is essentially conformal,

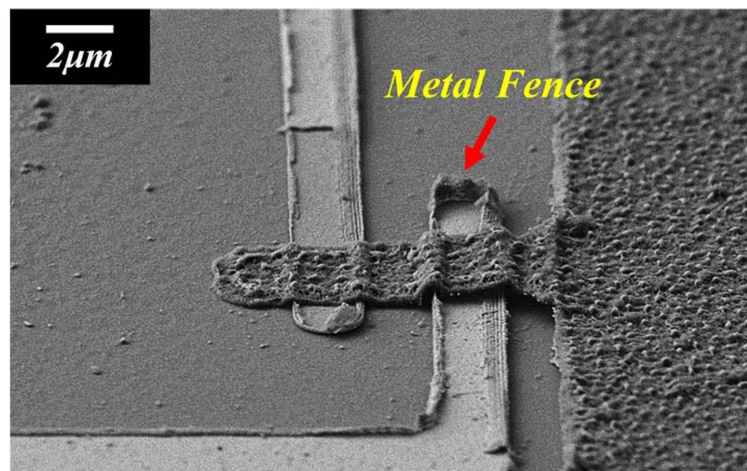


Figure 5.15: Metal fence from the conventional metal lift-off process.

the discontinuous surface topography created an extreme geometry in the SWNT film. This is a stress riser which led to premature mechanical failure of the cantilever. We have observed broken SWNT films near the metal fences after several switching events, as shown in Figure 5.16.

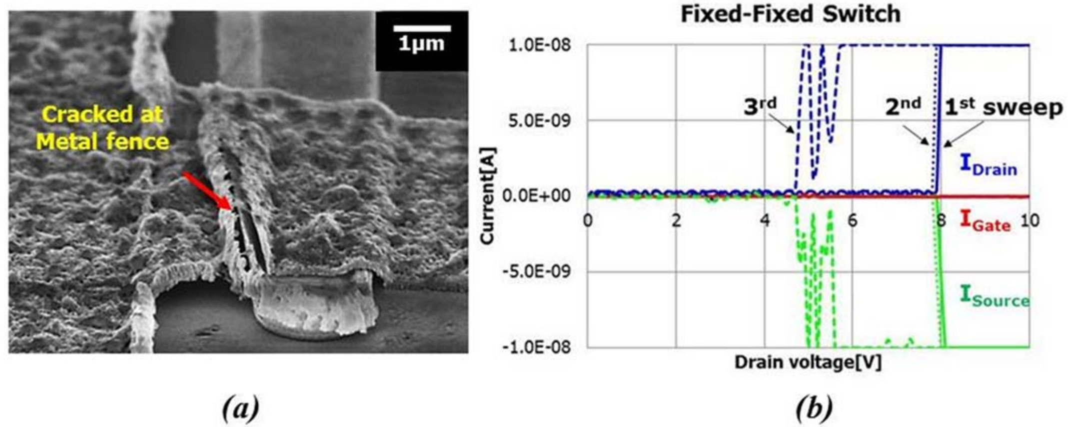


Figure 5.16: (a) SEM image of a cracked film at metal fence in our initial attempts and (b) I-V curves change after multiple switching operations.

Moreover, there was no gate oxide to prohibit shorting between the all-SWNT film and gate electrode. Figure 5.17 shows a schematic and I-V characteristic of our first 3-terminal device. The chromium parts after wet etching of gold on its top are used for the gate electrodes. In this case, we observed that the actuator may experience a second "Pull-in" event between the all-SWNT beam and gate electrodes as shown in Figure 5.17 (b).

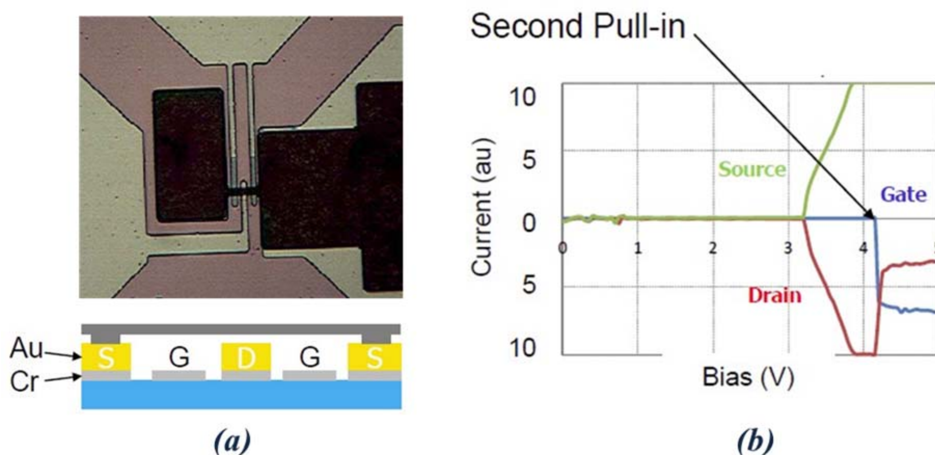


Figure 5.17: (a) First 3-terminal device and its schematic, (b) Pull-in Characteristic.

This occurs because the LbL deposition process produces a very conformal film, which means the air-gap between SWNT beam and conducting gate electrode is almost same as that between SWNT beam and drain electrode. Also, this design has a minor drawback that the wet etching process for removal of gold from gate electrodes is not easily controlled.

5.3.2. Metal Embedded Flat Substrate Process

We modified our design as shown in Figure 5.18. The main concept of new design is described as the metal fence-free planar electrode. It was formed by adopting an embedded metal process and an insulating film above the gate electrodes.

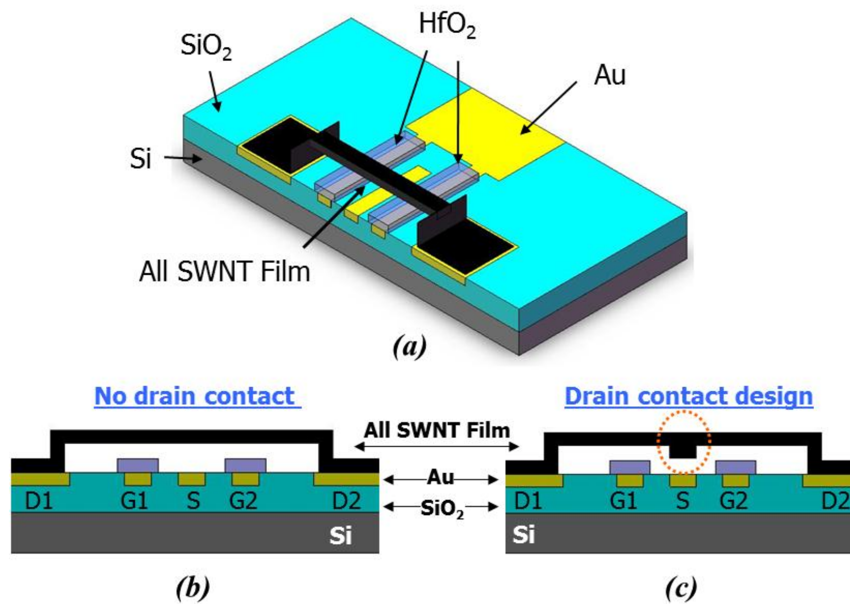


Figure 5.18: Modified 3-terminal switch structures; (a) overall structure, (b) a device without drain contact dimple, (c) a device with drain contact dimple.

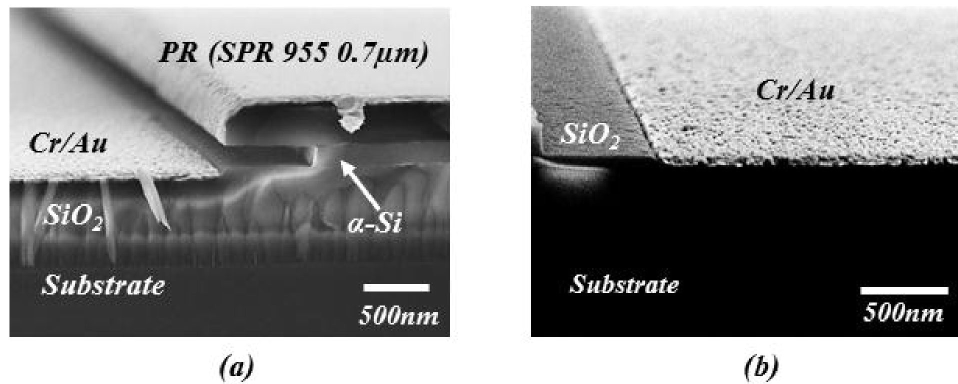


Figure 5.19: Cross-section SEM images of (a) a substrate after metal evaporation showing modified LOR Process, and (b) a substrate with the fence-free and flat embedded metal.

For a metal-fence-free and topographically flat substrate, we adopted an embedded metal process using a lift-off resist (LOR), as shown in Figure 5.19 (a). A 300 nm thick plasma enhanced chemical vapor deposited (PECVD) α-Si film was used instead of the LOR, since it can be isotropically dry etched in a more controllable manner than the typical wet-developed LOR processes. Prior to metal evaporation, the oxide was etched 100nm deep to form the embedded metal structure. After the lift-off process, the α-Si film was removed and a metal-fence-free and flat substrate was obtained, as shown in Figure 5.19 (b).

5.3.3. Modified Sacrificial Layer Etch Process

To minimize the stiction issue in the same manner of the 2-terminal switch fabrication, the α-Si was used as a sacrificial layer and removed by a dry etching process based on an SF_6 plasma. As discussed in the Chapter 4, the 2-terminal switch was

patterned by e-beam lithography and the widest beam was just 100nm. Therefore, the device release process was not very difficult. However, the 3-terminal switches are patterned by optical lithography using an i-line stepper, whose minimum patternable feature size is about 0.5μm. The free-standing beam becomes longer than the 2-terminal device. This implies that the film thickness and width should be increased to ensure a free standing structure after α-Si removal.

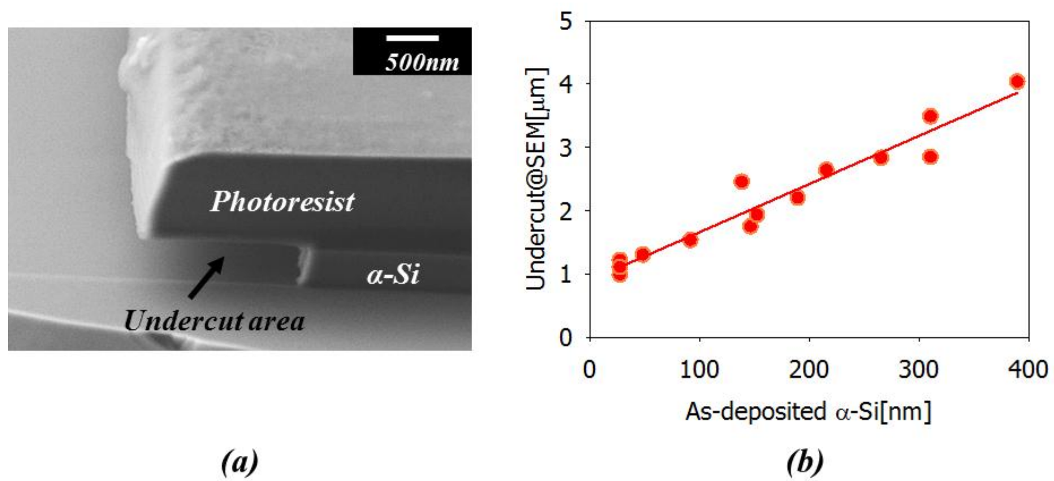


Figure 5.20: (a) Cross-section SEM image to show the undercut after etching of 310nm thick α-Si for 30 seconds and (b) Undercut length (SEM measurement) dependency on the as-deposited α-Si thickness.

As a result, a modified α-Si etch recipe should be found to get the larger α-Si undercut for the device release. From extensive experiments, a new α-Si etch recipe was found, which was able to get an etch rate of about 3.4μm per minute at 300 W power, 300 mTorr pressure, and 200 sccm SF_6 flow using the STS etch system as shown in Figure 5.20 (a). The undercut length of α-Si was investigated through the measurement of SEM images depending on the as-deposited α-Si thickness, as shown in Figure 5.20 (b).

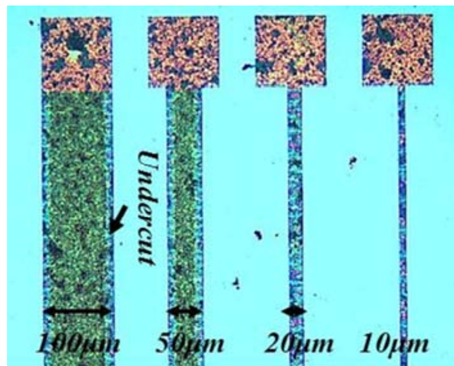


Figure 5.21: An optical microscope image of bar resistors to show the undercut after etching α-Si for 5 minutes with the modified recipe.

Also, Figure 5.21 depicts how much the undercut below the all-SWNT thin film was made after etching α-Si for 5 minutes with the modified recipe. Clearly, it appears that the α-Si was fully removed under the 20μm wide bar resistor. Therefore, the undercut would be more than 10μm per side. This is sufficient for our 3-terminal switch application.

5.3.4. Overall Process Flow

Figure 5.22 shows the overall process steps for the i-line stepper (Canon i3-2500) to make our 3-termial switches using a suspended all-SWNT film. To make fence-free electrodes, we had to modify typical two photoresist based process such as the LOR process. In this work, we used 300nm thick α-Si instead of LOR (Microchem, Inc.), because this α-Si can be removed isotropically by dry etching and it is more controllable than the LOR process which is based on wet etching. The starting substrate is prepared by depositing 300nm thick α-Si on 2um thick PECVD SiO_2 which was deposited on silicon.

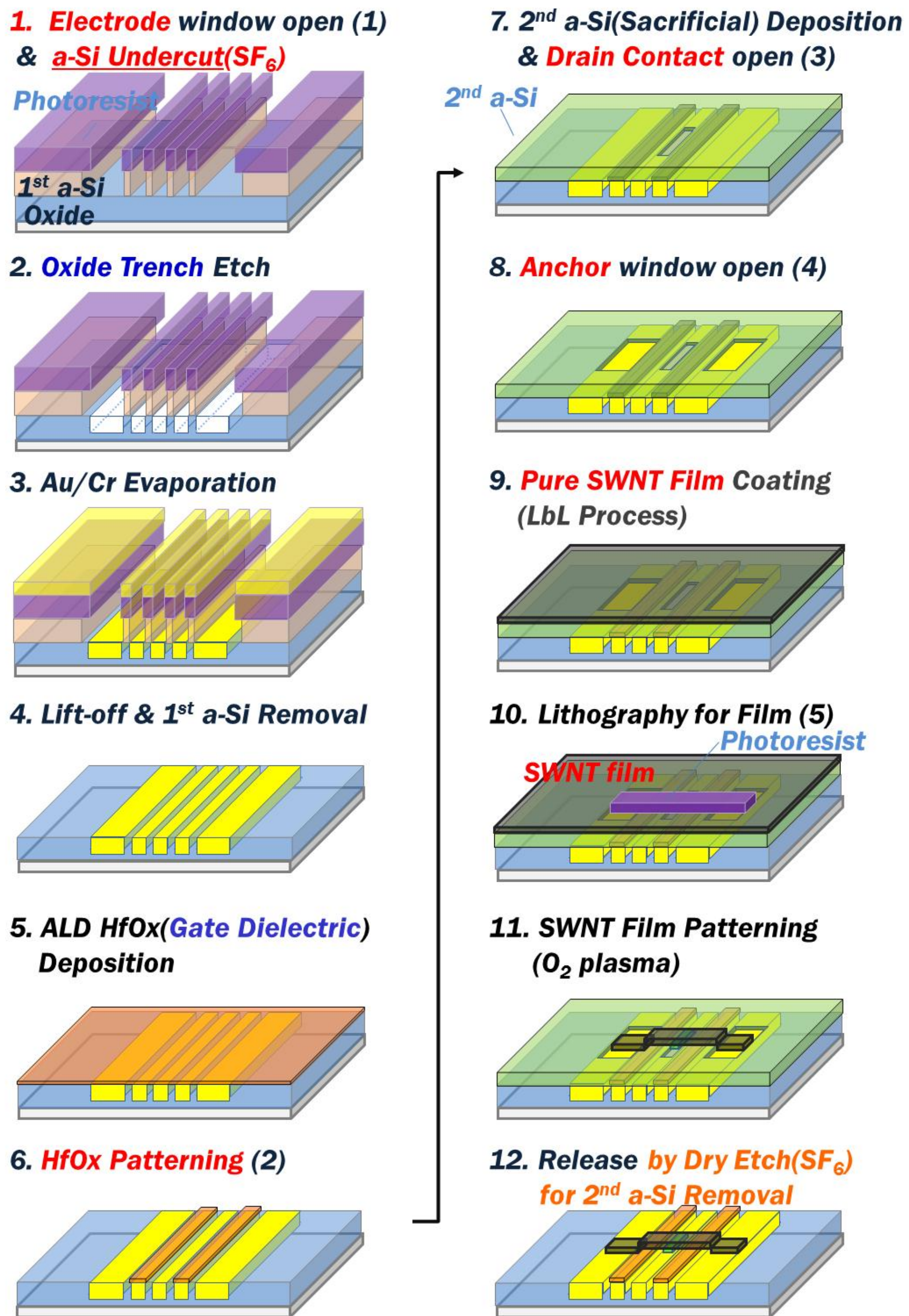


Figure 5.22: Overall device fabrication process flow.

First, the Cr/Au stacked gate electrode area is opened by lithography and the exposed α-Si is etched out by SF_6 plasma etch using the STS etcher (Model 320) at 300 W, 300 mTorr, and 200 sccm SF_6 flow for 1 minute. This etching is almost isotropic, so an undercut of about 300nm is made under the photoresist as shown in Figure 5.21. Next, 100nm thick silicon dioxide is etched out using the STS etcher at 150 W, 75 mTorr, and 50 sccm Ar flow, 25 sccm CF_4 flow and 50 sccm CHF_3 flow for 3 minutes and 30 seconds. Then the gold and chromium are deposited by e-beam evaporation, and then the wafer is soaked into acetone with sonication for 5 minutes for lift-off process. The remained α-Si is removed by SF_6 plasma etch using the STS etcher at 300 W, 300 mTorr, and 200 sccm SF_6 flow for longer than 15 minutes. Next, the gate electrodes are insulated with 10nm thick hafnium dioxide by atomic layer deposition (ALD). Hafnium dioxide was chosen as a gate insulator because its thickness is well controlled and we could expect lower pull-in voltage compared to the case of using silicon dioxide because its dielectric constant is about six times bigger than silicon dioxide [317].

The α-Si is deposited as a sacrificial layer by PECVD and the anchor regions are patterned by i-line stepper lithography. The thickness of α-Si needs to be well controlled because it determines the air gap between all SWNT film and gate electrode and eventually determines overall switching characteristics of our devices. Prior to depositing the all-SWNT film on the substrate, the α-Si is removed by dry etching using the STS dry etcher to make anchors. We also added an optional drain contact dimple to insure good contact between suspended all-SWNT thin film and drain electrode. Then the all-SWNT film is deposited on the device with LbL self-assembly process and it is patterned by i-

line stepper lithography and O_2 plasma etching using STS etcher at 100s W, 50 mTorr, and 100 sccm oxygen flow for 3 minutes. Finally, to release the all-SWNTs membrane, all of the α-Si under the patterned membrane is removed by dry etching using STS etcher at 300 W, 300 mTorr, and 200 sccm SF_6 flow for 10 to 30 minutes depending on the thickness of pre-deposited α-Si.

5.4. Device Performance

In this section, the characteristics of fabricated 3-terminal switches are discussed including pull-in and pull-out voltages. Also they are compared with theoretical models and the differences are discussed.

5.4.1. Pull-In Voltage Measurement Set-up

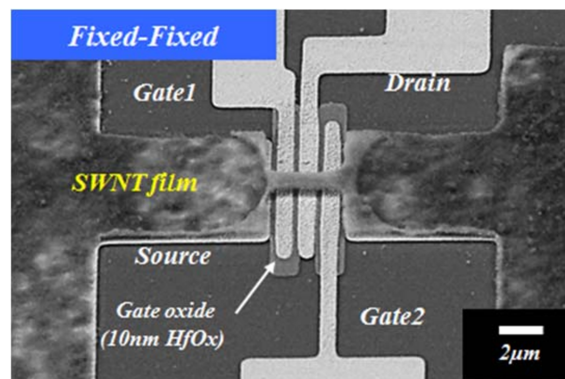


Figure 5.23: Fabricated 3-terminal Electromechanical Switch using all-SWNT thin film.

Figure 5.23 shows a fabricated 3-terminal electromechanical switch using an all-SWNT thin film. The fabricated device is 100nm thick, 1μm wide, and 3.45μm long. The α-Si sacrificial layer is about 50 nm thick, as shown in its schematic, Figure 5.24 (a). The width and spacing of gate and drain electrodes are about 0.75 μm and 0.3 μm, respectively. The all-SWNT beam is well free standing across the two anchor areas. The free standing beam would move up and down depending on the electric field between two gates and the beam.

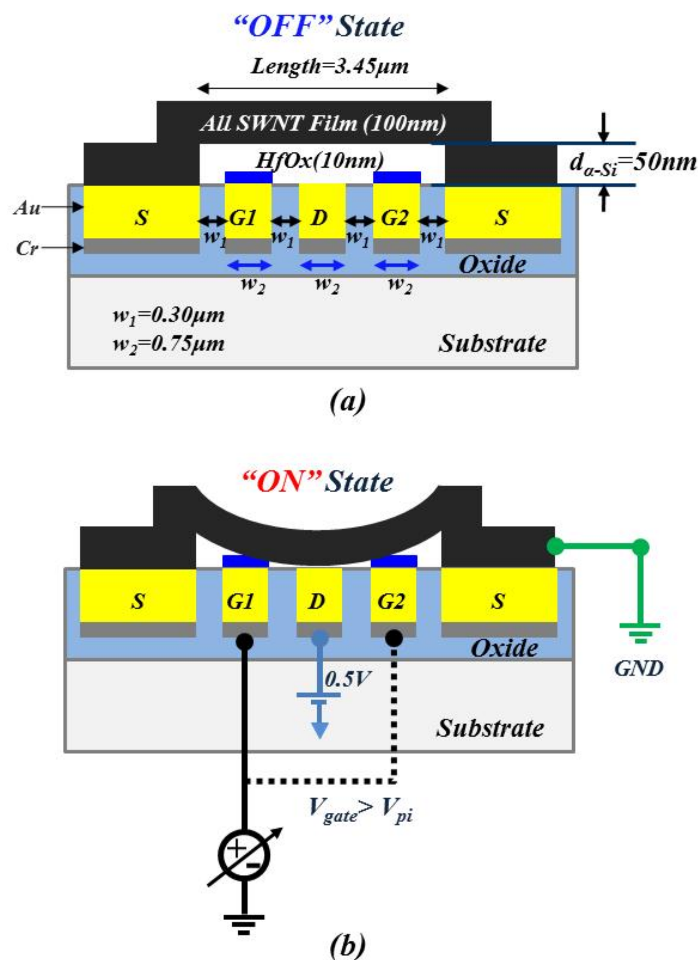


Figure 5.24: (a) Schematic of measured device, and (b) pull-in voltage measurement set-up.

Figure 5.24 (b) shows a schematic of pull-in voltage measurement set-up for the fabricated device. This 3-terminal switch operates with electrostatic force just as the two-terminal switch introduced in Chapter 4. Therefore, the pull-in voltage was measured by applying a dc voltage between the two gates and the beam. Increasing the bias voltage increases the electric charge on the beam, which results in an electrostatic force between two gates and the beam. When this force is large enough to overcome the mechanical restoring force in the beam, it snaps down.

However, no electric current path is established unless a dc voltage is applied on the drain contact because two gates are insulated with hafnium dioxide. Therefore, a dc voltage, 0.5V, was applied to see if the device works properly without disturbing the pull-in characteristic.

5.4.2. Two Input NAND Gate-like Operation

Unlike our 2-terminal device, the 3-terminal switch has two gates, which can be controlled independently. The functionality of our 3-terminal electromechanical device was checked by forcing different biases for each gate. This device behaves like a 2-input NAND gate, as shown in Figure 5.25. The free-standing all-SWNT membrane is electrically connected to the drain electrode when both gates inputs are biased higher than 4.2 V (High-High or HH). In contrast, when only one of two gates was biased and the other was grounded, (Low-High LH) or (High-Low HL), or both were held low (Low-Low or LL), no current was observed prior to gate oxide breakdown. Usually, for a NAND gate operation, the output should also be a voltage as response to a voltage input.

However, recall the current was through a resistive all-SWNT beam in Figure 5.25. Therefore, we could claim this operated like a NAND gate.

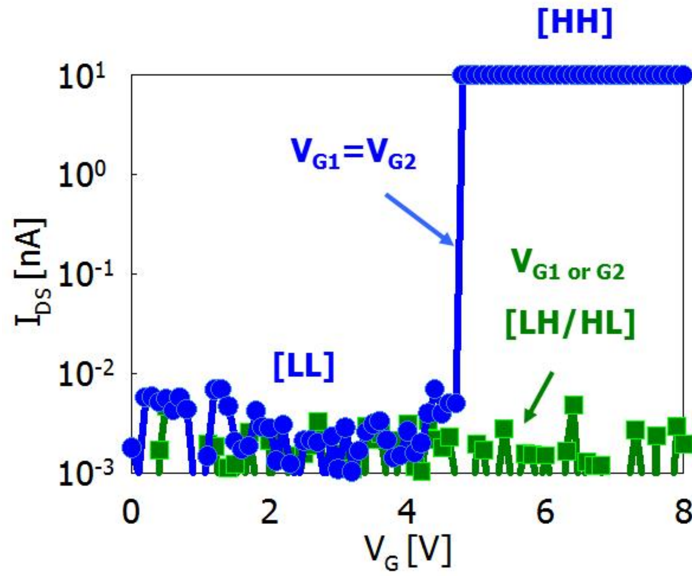


Figure 5.25: Measured Pull-In Characteristic of a device annealed at both 150˚C for 12 hours in 2-5mT and 300˚C for 2 hours in H_2/N_2 ambient.

5.4.3. Comparison with Pull-In Voltage Model

As reviewed in the chapter 2, when both gates of a 3-terminal MEMS switch are biased at the same potential, the spring constant (k) of all-SWNT beam can be modeled as below [20].

$$k_{3-terminal} = 125Ew\left(\frac{t}{l}\right)^3 \tag{5.5}$$

And the pull-in voltage can be estimated considering the effect of the insulating layer (ε_r, t_d) on both gates as below [20].

$$V_{PI} = \sqrt{\frac{4}{27}\frac{k_{3-terminal}}{\varepsilon_0 wW}\left(g_0 + \frac{t_d}{\varepsilon_r}\right)^3}\ . \tag{5.6}$$

where g_0, t_d, and ε_r are the air-gap, hafnium dioxide thickness and its relative dielectric constant, respectively.

Using equation 5.6, the pull-in voltage was calculated as a function of beam length and compared to the measured data with a fixed electrode and beam width (1μm) in the Figure 5.26. There is a clear discrepancy between measured data and model. In the Chapter 4, we saw that the contact surface roughness could considerably reduce the pull-in voltage of 2-terminal device due to the increased the effective capacitance in the parallel plate model by the larger effective contact area and the smaller effective air-gap.

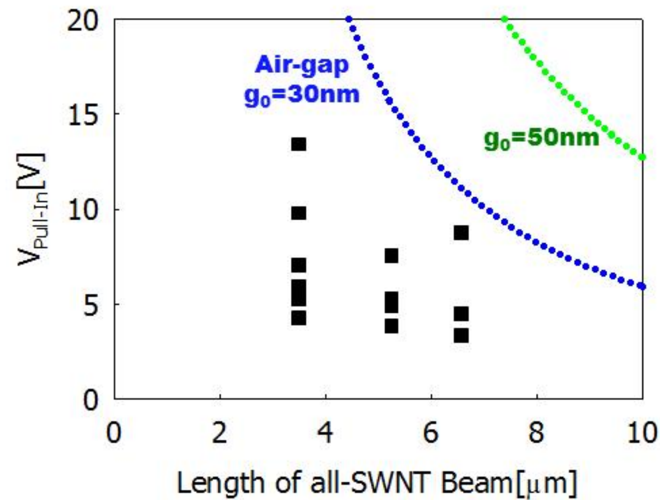


Figure 5.26: Comparison the measured data with the modified pull-in voltage model considering the contact surface roughness effect.

The contact roughness was mainly due to the gold diffusion at the interface with α-Si, even if the final process has performed with approximately no time delay and without a thermal treatment since α-Si was deposited on the substrate. In the 3-terminal devices, the gate electrodes are insulated with hafnium dioxide by atomic layer deposition. The surface roughness is not measurably different than the as-deposited gold. However, the surface roughness of all-SWNT film with 10-cycle deposition was about 26.7nm and linearly proportional to the total number of deposition cycles. If the bottom of the film is similarly rough, the discrepancy may still be explained by increasing the capacitance. Using the Kogut model [70], the ratio of pull-in voltage reduction due to surface roughness was estimated in case of 30nm and 50nm of air-gap as shown in Figure 5.27.

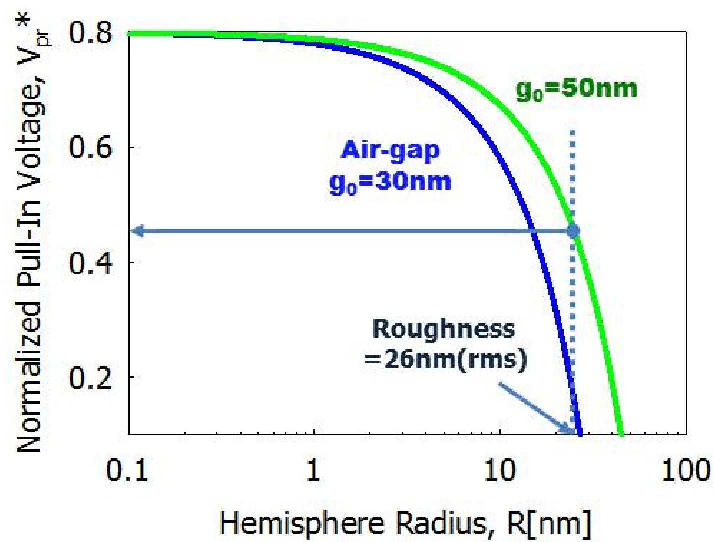


Figure 5.27: Normalized pull-in voltage depending on the surface roughness from Kogut model [70].

Although the thickness of sacrificial α-Si layer (50nm) determines the air-gap, some all-SWNT beams may be somewhat sagged down due to the intrinsic and/or extrinsic stresses, which results in smaller air-gap. Therefore, the pull-in voltage reducution in case of 30nm of air-gap was also considered. Assuming that the bottom and top surface of all-SWNT film have an identical roughness for the worst case, the pull-in voltage may be reduced up to about 60% compared to the smoothly surfaced device with 50nm air-gap. This depicts that the variation of pull-in voltage could be significantly increased when the surface roughness is larger than 10nm and/or smaller air-gap. Even though it seems very unlikely that the bottom of the film would become rougher as the film is thicker, the precipitates and agglomerates in the first layer may be included in the bottom surface of the pure SWNT films.

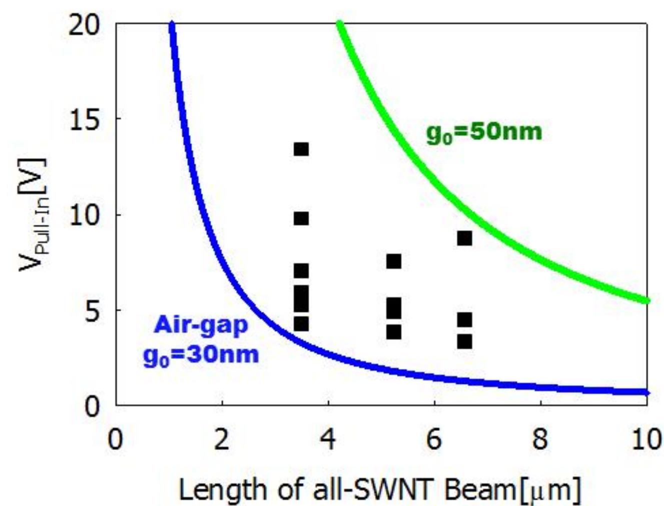


Figure 5.28: Normalized pull-in voltage depending on the surface roughness from Kogut model.

Therefore, depending on their sizes and numbers, the bottom surface roughness of pure SWNT film might be ranged from a few nanometers to tens of nanometers and this approach would be still useful to explain the pull-in voltage variations.

Now, taking into account the film surface roughness, the pull-in voltage model is simulated and compared with the measurement data as shown in Figure 5.28. The measured data are located between 30nm and 50nm air-gap lines and appear to fit reasonably well. However, as mentioned, this was possible because we had used several critical assumptions. Basically, the all-SWNT film is not a uniform and isotropic material. This causes an error when estimating the stiffness. Moreover, the surface roughness effect should be approached as a statistical problem because the SWNT bundles and unexpected agglomerates would be randomly distributed and each of them would give a different effect on the overall pull-in voltage.

5.4.4. Hysteresis between Pull-In and Pull-Out Voltages

As introduced in the Chapter 4, the MEMS/NEMS devices may experience a large hysteresis between pull-in and pull-out voltages due to the surface forces such as van der Waals force and short range forces [21]. Especially, this may become worse in the devices with smaller spring constant, which have a thinner, longer and narrower free-standing beam. For the same lithography, a 3-terminal device has longer beam than 2-terminal device due to two additional gates for actuation. Figure 5.29 shows the hysteresis between pull-in and pull-out voltages of a 3-terminal switch. The measured hysteresis is more than 2 volts, which is much larger than the 2-terminal switches.

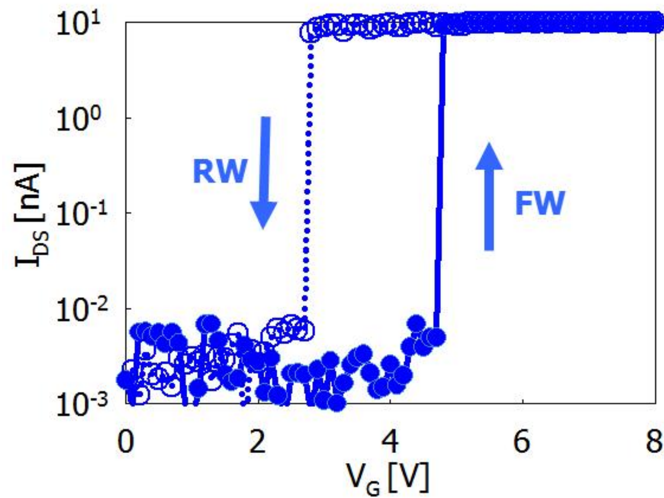


Figure 5.29: Hysteresis between pull-in and pull-out voltages of a fully-annealed 3-terminal switch with multiple measurements.

This difference may be due to the increased gold contact surface roughness if the all-CNT film coats the rough gold surface conformally, thereby increasing the contact area. The roughness of the gold surface is shown in Figure 5.30. Each bar is filled with an AFM scanned image and its height is depending on the root-mean-square (rms) surface roughness. Also, for fair comparison, the same sample was prepared, processed and measured. Therefore, the measure data reflect cumulative effect from as-deposited to fully annealed states. The surface roughness of as-deposited gold was about 0.5nm. However, it is increased to 1.2nm in a day and 5.8nm in three days after α-Si deposition. Post deposition thermal treatments, such as those used to reduce the CNT film resistivity, also have a marked effect on roughness. It increases to 9.9nm after a 150˚C, 12hour anneal at 2-5mT and jumped to 26.3nm after the 300˚C, 2-hour anneal in a H_2/N_2 ambient.

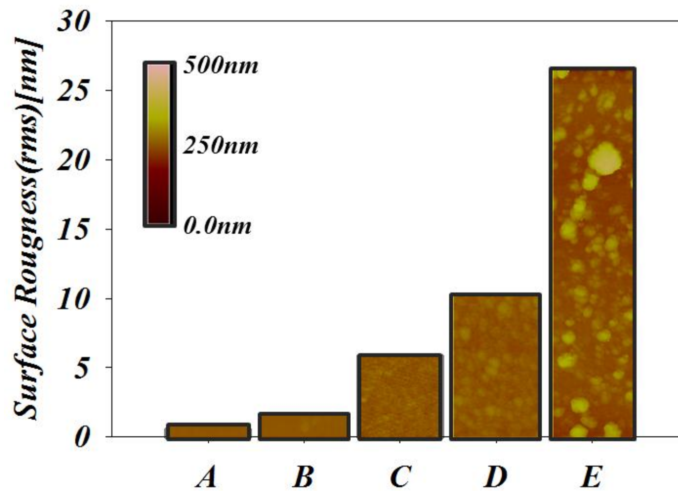


Figure 5.30: Increasing cumulative AFM surface roughness (rms) depending on the number of days after α-Si deposition and thermal treatments (A=pure gold, B=a day after α-Si deposition, C=3 days after α-Si deposition, D=150˚C for 12hours annealing at 2-5mT, E=300˚C for 2hours annealing at H_2/N_2 ambient.).

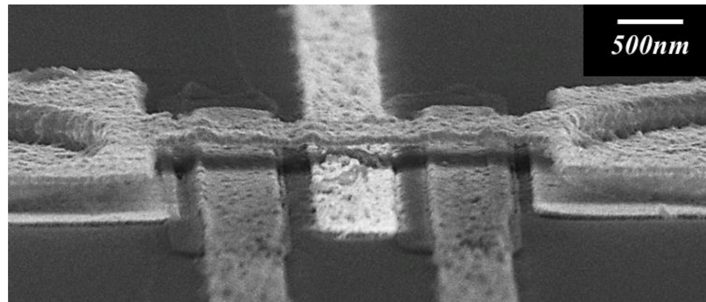


Figure 5.31: An SEM image of 3-terminal device after fully annealed.

It took less than a day after α-Si deposition to complete 2-terminal switch fabrication. However, in case of the 3-terminal switch, it typically takes more than 4 days because the annealing process is critical to improving the electrical properties of the beam. Figure 5.31 shows a low-angle SEM image of a fully annealed device after release to see the drain contact surface texture. As expected, the drain contact surface looks very rough. This increased contact surface roughness helps lowering pull-in voltage by increasing

total actuating area, but it also increases the possibility of stiction and pull-out voltage due to the increased van der Waals force and short range forces [21, 70].

5.5. Process and Device Issues for Device Applications

In this section, yield-related issues are discussed. This includes the intrinsic problem related to the quality of SWNT dispersions to accidental problems such as Ni impurities. All of the issues discussed in this section should be improved or resolved to get a sufficient yield for demonstrating circuit operation with all-SWNT thin film 3-terminal switches.

5.5.1. Agglomerates in Deposition Process

Some of SWNTs in each dispersion aggregate into bundles or ropes or even bigger agglomerates due to the strong Van der Waal interactions between SWNTs [286], as shown in Figure 5.32, when they are not sufficiently functionalized or where the net surface charge distribution is substantially different. The SWNTs agglomerates are randomly generated and if they deposit on the beam area, the beam may not be released after α-Si etching process as well as the device characteristics will be changed in a non-expectable way, even if the beam could be released. Furthermore, the inhomogeneity of the material represented by these defects could give rise to stress gradients than alter device operation.

There are two possible routes to forming SWNTs agglomerates. The first is

insufficient functionalization of the SWNTs. The SAP oxidation process in particular, has considerable variance in the as-produced materials. We believe that this is likely due to variations in the synthesis of SAP, the age of a particular batch, and the amount of moisture still in the SAP. The SAP is more effective when thoroughly dried, but decomposes more rapidly during SWNTs functionalization, causing the reaction mixture to flash out of the reaction vessel. Another factor that may impact the resulting charged SWNTs is the presence of organic byproducts from the recombination of radical intermediates or hydrolyzed SAP. These imperfections in the functionalization process would facilitate the agglomeration of SWNTs. To be ultimately successful, one must investigate ways to precisely prepare SAP for functionalization, and to limit and effectively remove byproducts from the functionalized SWNTs.

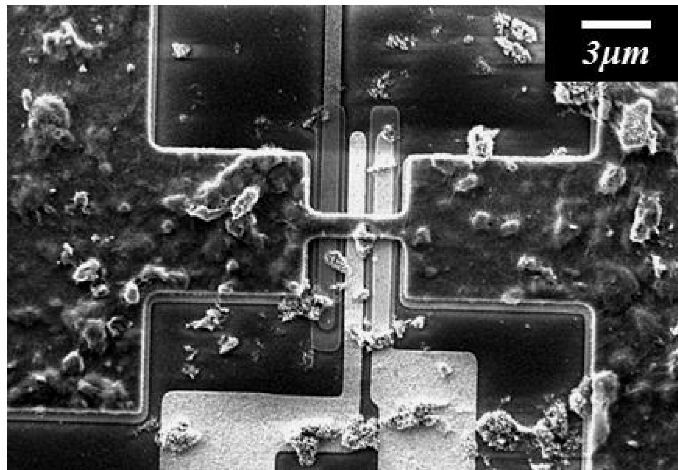


Figure 5.32: An SEM image of the SWNT agglomerates formed during deposition process.

The second possible cause is due to the insufficient rinsing and drying of the substrate in each dipping cycle. This can exacerbate the agglomeration process by degrading the functionality of both dispersions. Frequent sonication and centrifugation of the dispersions during deposition process may help to reduce agglomerate formation and deposition on the substrate.

5.5.2. Wrinkles due to Nickel Impurities

Normally, the SWNTs deposit as a uniform film on the substrate as explained in the Section 5.2.2, except for randomly distributed agglomerates. However, wrinkles were observed after patterning an all-SWNT film, which was deposited from a set of dispersions prepared with microwave reactor as shown in Figure 5.33. These strange wrinkles were discovered all over the substrate, and were barely distinguishable in the as-deposited film.

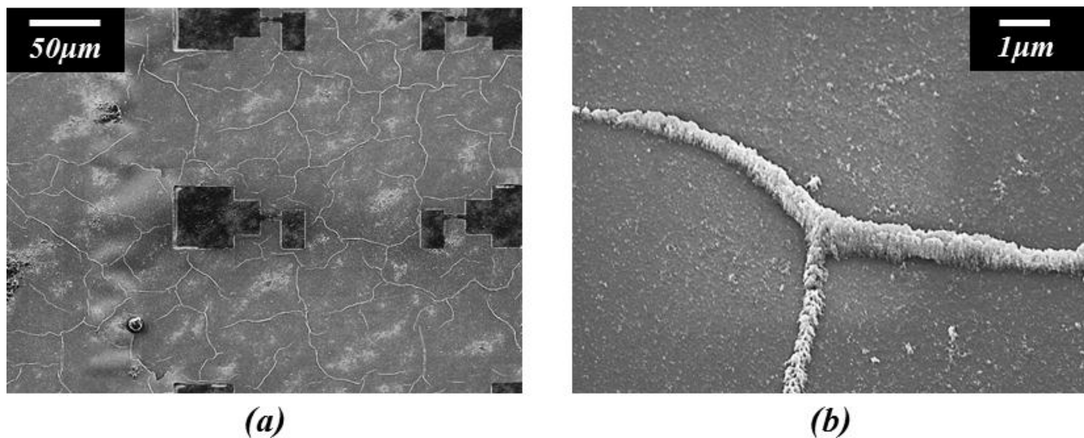


Figure 5.33: (a) An SEM image of the SWNT wrinkles formed during deposition process, and (b) a magnified wrinkle.

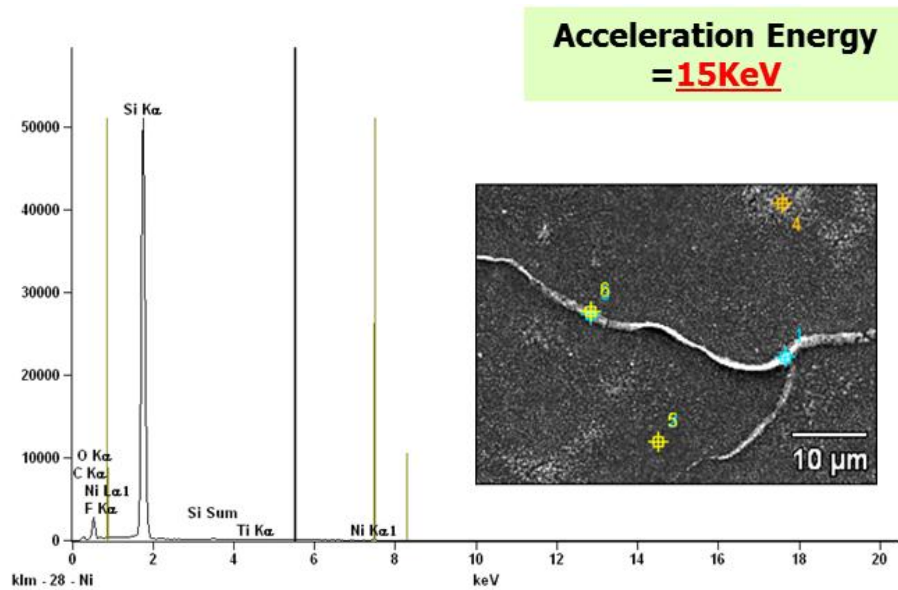


Figure 5.34: An energy dispersive spectroscopy (EDS) area scan mode result on the "Wrinkle" area.

Element	Net Counts	Net Counts Error	Weight %	Weight % Error	Atom %	Atom % Error
C	2989	+/- 52	10.22	+/- 0.18	18.59	+/- 0.32
O	16921	+/- 145	19.64	+/- 0.17	26.83	+/- 0.23
F	778	+/- 119	0.66	+/- 0.10	0.76	+/- 0.12
Si	490314	+/- 1695	68.81	+/- 0.24	53.56	+/- 0.19
Ti	266	+/- 68	0.12	+/- 0.03	0.05	+/- 0.01
Ti	0	+/- 61	---	---	---	---
Ni	423	+/- 72	0.56	+/- 0.09	0.21	+/- 0.04
Ni	650	+/- 116	---	---	---	---
Total			100.00		100.00	

Table 5.3: Detected atoms list from an energy dispersive spectroscopy (EDS) area scan mode result on the "Wrinkle" area.

The wrinkles were analyzed with energy dispersive spectroscopy (EDS) installed on the JEOL6500 SEM system. Initially, an area survey scan was performed to determine the species present as shown in Figure 5.34. From the EDS area mode scan, a small amount of titanium (Ti) and nickel (Ni) were detected as 0.05 atomic percent and 0.21 atomic percent, respectively, as listed in the Table 5.3.

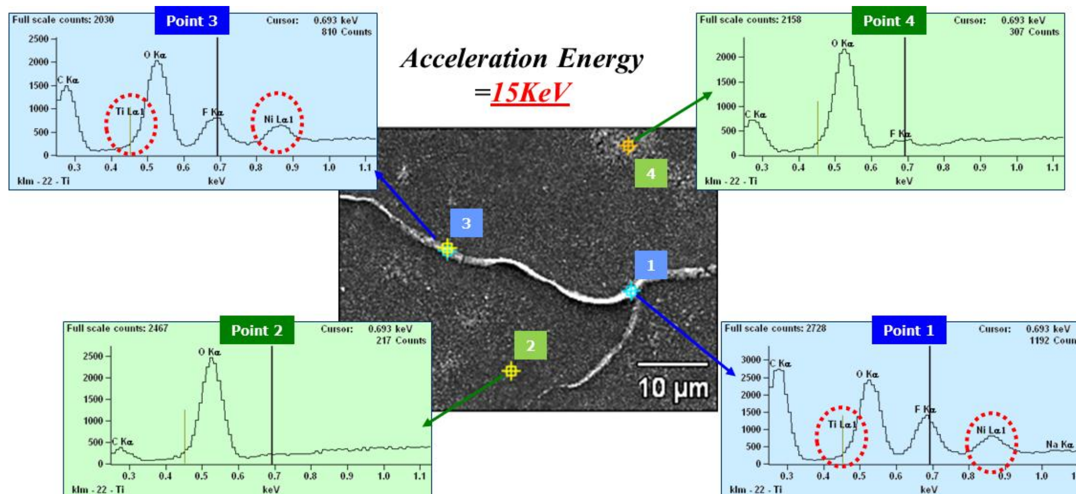


Figure 5.35: An energy dispersive spectroscopy (EDS) point scan mode result on the "Wrinkle" area.

	C	*O*	*F*	*Na*	*Si*	*Ti*	*Ni*
Base(1)_pt1	47.62	18.90	5.48	0.03	26.79	0.29	0.89
Base(1)_pt2	14.84	27.16			58.00		
Base(1)_pt3	39.32	18.56	3.26		38.13	0.23	0.49
Base(1)_pt4	26.73	22.91	0.53		49.83		

Table 5.4: Detected atoms list in atomic percent from an energy dispersive spectroscopy (EDS) area scan mode result with 15KeV acceleration energy on the "Wrinkle" area.

As shown in the Figure 5.35, the point mode scan was performed to locate the Ti and Ni. Four points were chosen, two points on the wrinkle and two points far from a wrinkle. All points on the wrinkle had the Ti and Ni. In contrast, these elements were not found for the two points outside of wrinkle. From these results, it is believed that the Ti and Ni formed the strange wrinkles. Ni is used as a catalyst in the CVD growth. Therefore, the Ni might attract nearby SWNTs during the deposition, resulting in the formation of wrinkles. This implies the Ni impurity in SWNT dispersions should be removed to get a "Wrinkle-free" SWNT film.

The source of the nickel was considered next. Possibilities include the SWNT production, functionalization, or deposition. As introduced in the Chapter 1, the CNTs can be produced by CVD growth using a wide variety of catalytic species such as Fe, Co, and Ni. These SWNTs were purchased from Cheaptubes.com (>90% purity, 5-30 μm length, 1-2 nm outside diameter), which were prepared by the combustion chemical vapor deposition (CCVD) process [318]. In this process, Cobalt was used as a catalyst. Moreover, in the film deposition process, only milli-Q water was additionally used for rinsing the substrate. Therefore, these two can't be the source of titanium and nickel. Most SWNTs functionalization was done manually. Interestingly, the negatively functionalized SWNTs dispersion was prepared with the microwave reactor (CEM Discover LabMate microwave synthesis system). Other batches that were prepared by heating in a beaker did not show the contamination.

5.5.3. Unfused SWNT Bundles

In the Section 5.4, the switching operation of a fully-annealed device was demonstrated. The transition from off-state to on-state is very abrupt, essentially discontinuous in the annealed device, corresponding to zero subthreshold swing. However, initially, this was not true for the unannealed devices as shown in Figure 5.36. It is believed that upon release some SWNT bundles deflect from the bottom of the film, and so have a reduced air gap. As a result, these discrete whiskers pull in at a lower voltage. This can be resolved by fusing the bundles through the previously described two step thermal treatments prior to release, as shown in Figure 5.39.

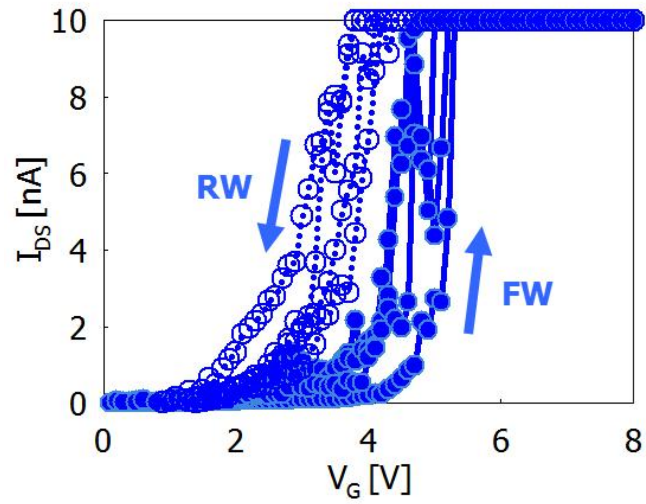


Figure 5.36: I_{DS}-V_G characteristics under repeated switching test of a fresh device.

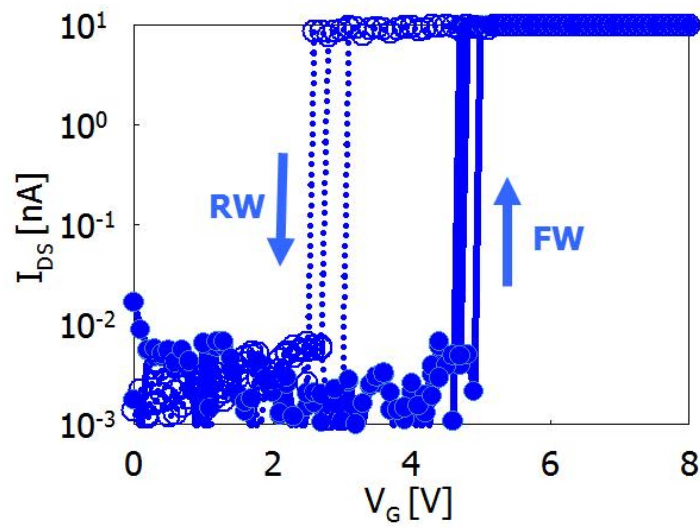


Figure 5.37: I_{DS}-V_G characteristics under repeated switching test of a fully-annealed device.

5.5.4. Extrinsic Residual Stress Induced by Sacrificial Layer

To minimize the device yield loss during wet etching of the sacrificial layer due to "stiction", a dry etch process using α-Si as the sacrificial layer was adopted in this work. However, uncontrolled film stress leads to snap down, especially in longer devices than 6μm, as shown in Figure 5.38 (a). The PECVD silicon dioxide and the α-Si induce compressive stress because they are deposited only on the top wafer surface. Then, tensile stress would be created in the all-SWNT beam. To see how stress acts on the substrate, the wafer curvature was measured with a profiler (KLA Tencor P-16). When the α-Si is removed, the wafer becomes less concave up. The difference of curvature before and after etching α-Si would be negative (a blue line in Figure 5.38 (b)).

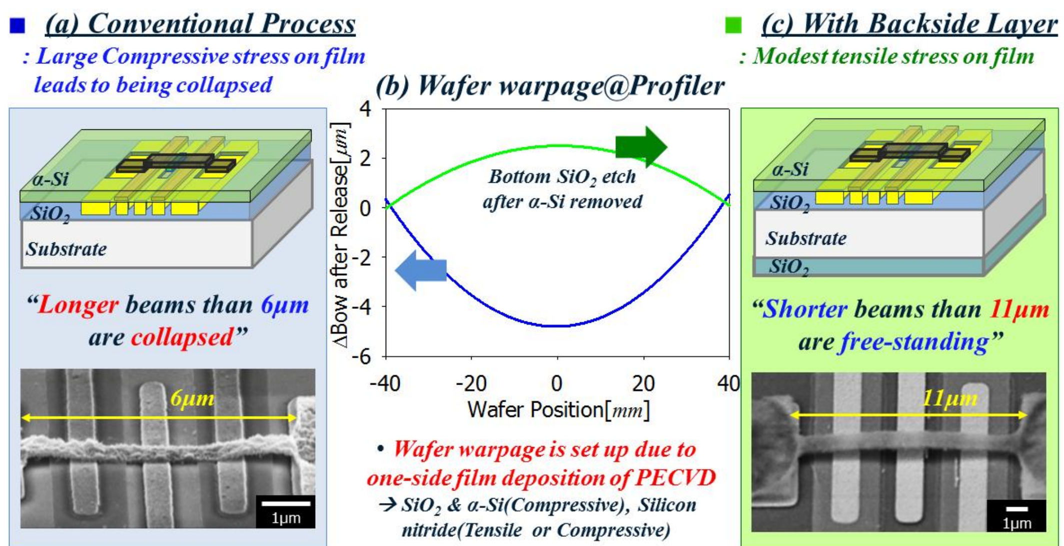


Figure 5.38: Wafer stress control with backside PECVD oxide deposition to improve the free-standing beam yield after etching sacrificial layer, (a) a conventional process by only front side PECVD silicon dioxide deposition, (b) a wafer warpage change after etching α-Si and/or back side silicon dioxide from profiler (KLA Tencor P-16) measurement, (c) a modified process to improve the device yield.

Therefore, the released beams are prone to collapse rather than be free standing. The longer beams are more vulnerable due to their smaller spring constant. To mitigate this problem, we coated thin PECVD SiO_2 on the backside of substrate before depositing the all-SWNT film to compensate the stress. After all-SWNT film was deposited and patterned, the backside SiO_2 was removed then the device was released. In this case, slightly compressive stress may be induced in the film as shown in Figure 5.38 (b), which would help the SWNT beam to be free standing even in long devices as shown in Figure 5.38 (c). Up to 11μm long beams could be free standing. However, the α-Si as a sacrificial layer is still a highly compressive material. The compensation process described here uses the difference in two large numbers to set the stress in the beam. To get a fundamental improvement in reproducibility, an effort to find another sacrificial layer with very low stress is required.

5.5.5. Enhanced Gold Diffusion at the a-Si Interface during Thermal Treatments

The hysteresis between the pull-in and pull-out voltage for a 3-terminal MEMS switch was larger than 2 volt as discussed in the Section 5.4.4, in marked contrast to the 2-terminal switch. From the mechanical properties measurements, it turned out that the stiffness of the aligned-composite SWNT film and all-SWNT film is almost equivalent. Therefore, the hysteresis is mainly determined by van der Waals force and other short range forces as described in the chapter 4. There is one major difference in the device fabrication processes, namely the annealing process needed to improve the electrical and mechanical properties of all-SWNT film. In case of 2-terminal device fabrication with

aligned-composite SWNT thin film, the α-Si deposition and device release process were done with almost no time delay, often completed within one day. However, for 3-terminal devices, it took three days to complete its fabrication process including all-SWNT film deposition and thermal treatments after α-Si deposition. This time delay after α-Si deposition and thermal treatments facilitate the gold diffusion at the interface with α-Si. Gold diffusion into α-Si is much faster at high temperature than at room temperature. Moreover, near the eutectic point (~360˚C) for the binary system of gold and silicon (Figure 5.39) [319], the liquid Au-Si alloy could be wetting the silicon surfaces [320]. As a result, the surface roughness of gold electrodes is expected to be much worse than that of our 2-terminal device.

Figure 5.40 shows the SEM images of gold electrodes before and after α-Si etching for device release. All SEM images were taken after fully annealed with 150˚C for 12 hours at vacuum and 300˚C for 2 hours in the H_2/N_2 ambient with a flow rate of 10 sccm for each.

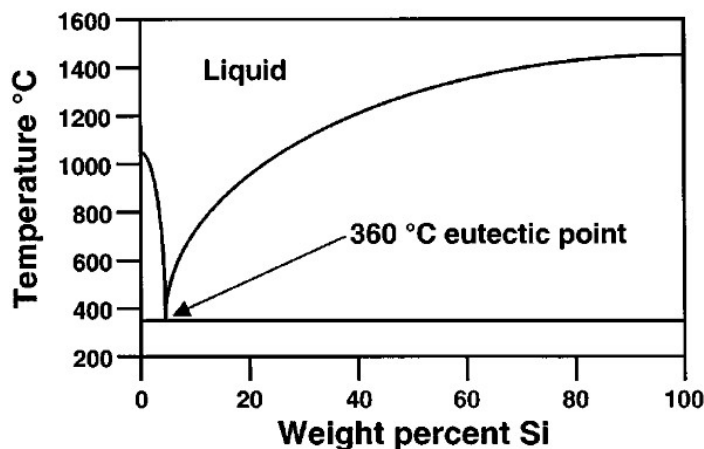


Figure 5.39: The phase diagram of the Au-Si binary system; Reproduced from [319].

While annealing the substrate, the α-Si reacted with the gold and made a Au-Si alloy as shown in Figure 5.40 (a). As a result, lots of "bubbles" on the gold electrodes were formed as shown in Figure 5.40 (b). Moreover, some of Au-Si alloy flowed out of the gold contacts as shown in Figure 5.40 (b) and (c). The Au-Si alloy was not removed by SF_6 plasma etching of α-Si. To verify the composition of this material an EDS analysis was performed as shown in Figure 5.41. The EDS spectrum in Figure 5.41 (a) is from the clean SiO_2 area. This indicates some carbon, but mostly SiO_2. In contrast, the EDS spectrum from the affected area in Figure 5.41 (b) depicts 6.2 atomic percent of gold as well as some carbon and SiO_2.

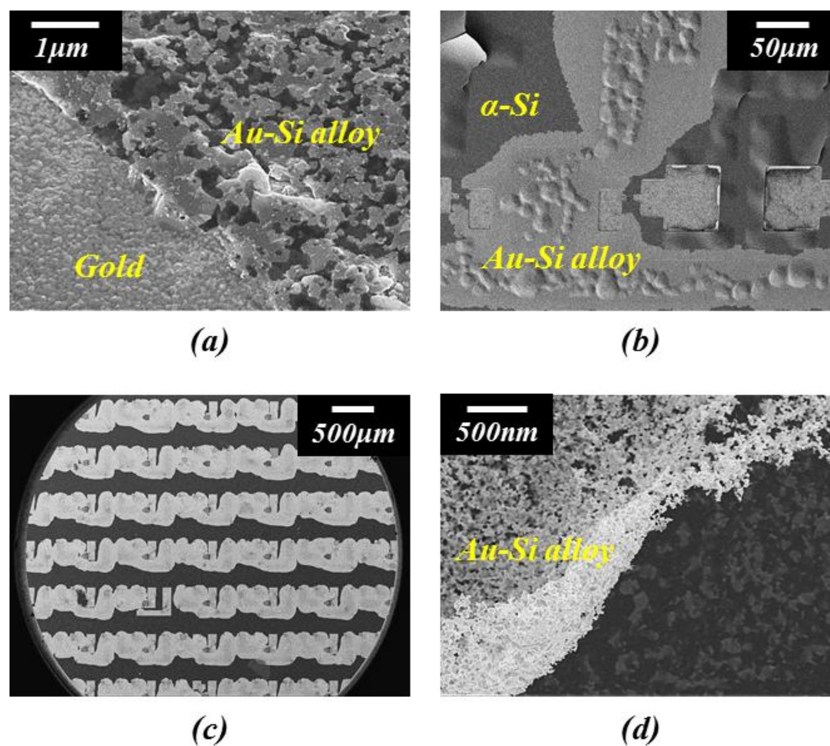
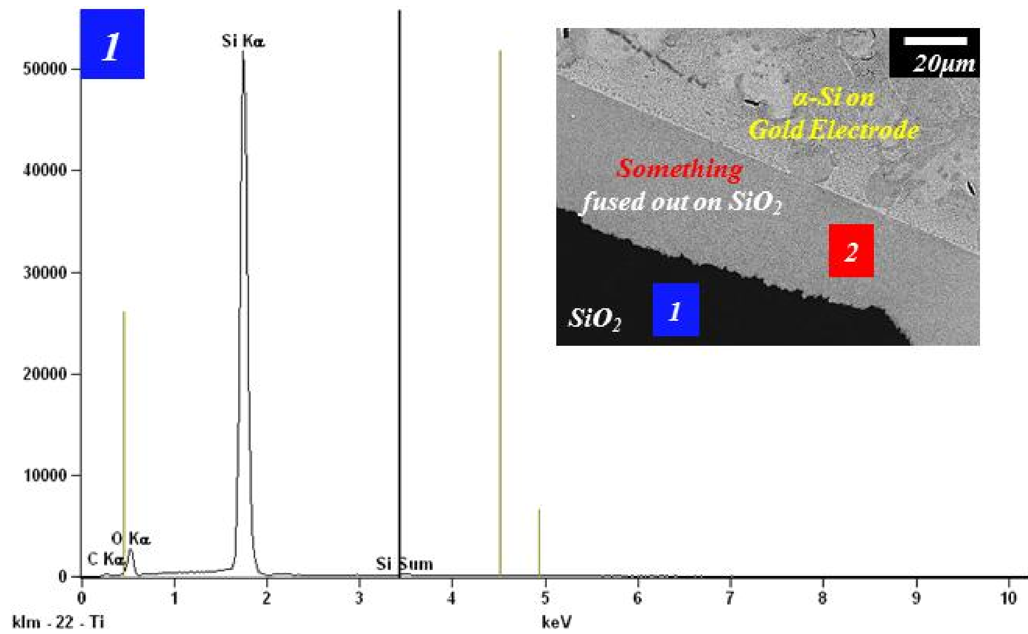
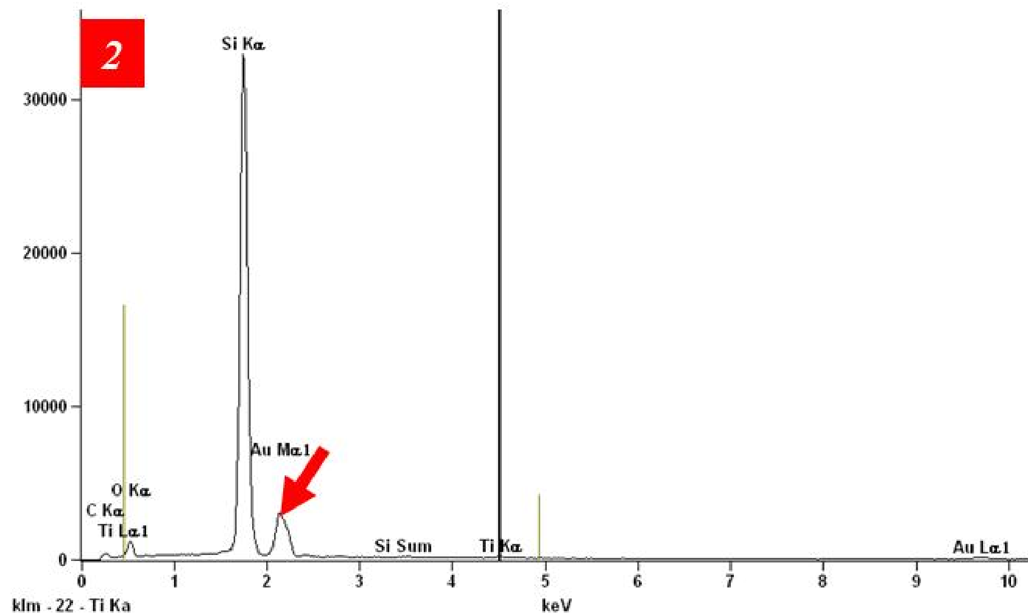


Figure 5.40: SEM images of gold electrodes before (a, b) and after α-Si etching for device release (c, d).



(a)



(b)

Figure 5.41: EDS analysis with 15KeV acceleration energy on the fused-out material from the gold electrode (1-SiO_2, 2-Fused-out material from the gold electrode).

Taking into account the penetration depth of the 5KeV electrons, the atomic percent of gold in the top layer is increased to 29.5% as listed in Table 5.5. Therefore, this material is a Au-Si alloy as expected. Depending on the anneal temperature, this alloy formation is increased and the α-Si surface would be much rougher than the unannealed α-Si surface. To reduce this effect, we should replace the gold electrode with some other metal such as palladium or platinum.

Element	*Net Counts*	*Net Counts Error*	*Weight %*	*Weight % Error*	*Atom %*	*Atom % Error*
C	7322	+/- 89	3.71	+/- 0.05	21.98	+/- 0.27
O	8096	+/- 123	5.80	+/- 0.09	25.81	+/- 0.39
F	746	+/- 117	0.48	+/- 0.08	1.81	+/- 0.28
Si	16887	+/- 241	8.24	+/- 0.12	20.87	+/- 0.30
Au	53037	+/- 488	81.77	+/- 0.75	29.54	+/- 0.27
Total			100.00		100.00	

Table 5.5: Detected atoms list in atomic percent from an energy dispersive spectroscopy (EDS) area scan mode result with 5KeV acceleration energy on the "Something fused-out" area.

5.6. Conclusions

An all-SWNT film was deposited through LbL self-assembly without use of a copolymer, resulting in 75% reduction of resistivity compared to our previous composite film with copolymer, without the need for CNT alignment. The deposited film thickness could be well controlled by changing the number of dipping cycles. Moreover, we demonstrated that 3-terminal MEMS switch built with this all-SWNT thin film behaved like a NAND gate. Through thermal treatments, its on- and off-current ratio could be dramatically improved as well as the electrical properties of the all-SWNT film. This 3-

terminal MEMS switch built with the all-SWNT film is believed to be a very promising device for low power digital logic applications, if yield related issues are resolved.

CHAPTER 6: COVENTORWARE SIMULATIONS

6.1. Overview

In this chapter, the process dependency of electrostatic MEMS switches will be discussed through a finite element analysis (FEA) using a commercial MEMS device simulation software (CoventorWare^{TM}). The pull-in voltage and fundamental resonant frequency were simulated as a function of the thickness and width of a movable beam, air-gap and gate overlap area. This simulation data can be used as a reference in designing 3-terminal fixed-fixed beam MEMS switches.

6.2. CoventorWare 2010 Overview

CoventorWare consists of several software tools for designing and simulating MEMS and microfluidics devices. This includes a system-level design approach using "ARCHITECT", and a physical design approach using "DESIGNER" and "ANALYZER" This section will provide a description of the operation of each of the tools. This information is taken from the CoventorWare 2010 Manual; www.coventor.com. Figure 6.1 depicts the overall design flow in CoventorWare. In this work, the latter approach was elected because the "DESIGNER" and "ANALYZER" modules support a manufacturing-aware physical design flow. The simulation procedure mimics the typical MEMS manufacturing process. Therefore, the first step in DESIGNER is to draw a 2-dimensional layout with the layout editor. The solid modeler then uses the layout to build

a 3-dimensional model with the layer stack information from the process editor. The software then generates a mesh. Depending on the physical parameters to be simulated, the user can select one of provided solvers such as the electrostatic property solver (MemElectro) based on the 3-D boundary-element method (BEM), the mechanical property solver (MemMech) based on the 3-D finite-element method (FEM) and the electrostatic-mechanical property coupled solver (CoSolveEM). In this section, the key features of these three solvers are briefly summarized.

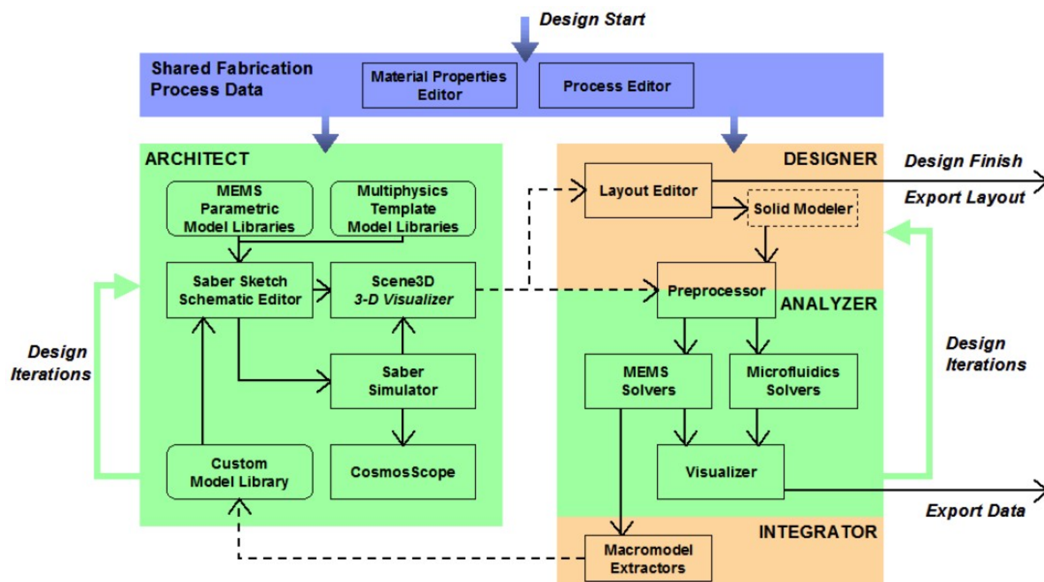


Figure 6.1: Overall design flow in the CoventorWare ; Reproduced from [321].

6.2.1. MemElectro

By default, MemElectro solves the electrostatics problem with the constraint that the net charge is zero, which is done by adjusting the applied voltages by a constant. This

corresponds to the physical situation of connecting conductors to a battery and letting the potential at infinity float. Under this constraint, the problem of finding the capacitance of a single conductor with respect to infinity is meaningless. Electrostatic problems with the constraint that the potential is zero at infinity may be solved with MemElectro by setting the environment variable MEMCAP_0V_INFINITY. The MemElectro solves the Laplace equation in a single-layer form of Gauss' law for the surface charge "q", given an applied potential "V", according the following equation,

$$V = \int_S \partial SPq \tag{6.1}$$

where P is the coulomb interaction between surface points. Solving this equation with a BEM leads to a discrete form where the linear system is dense. Consequently, the system matrix must be made sparse, or else the computation cost will be prohibitive. There are several sparsification techniques to be found in literature. MemElectro uses the pre-corrected fast Fourier transform algorithm [322].

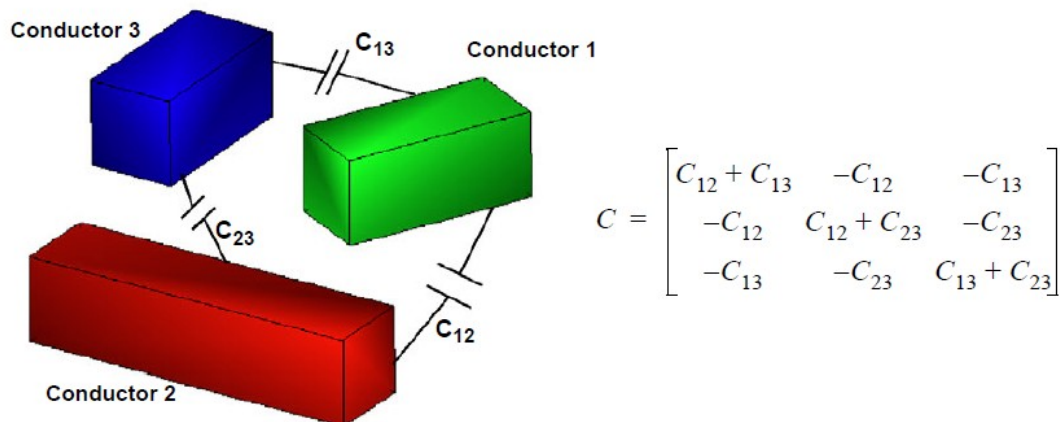


Figure 6.2: Representation of capacitance matrix for three conductors ; Reproduced from [321].

This approach approximates the far field BEM panels by point sources on a regular grid. Because these influences are regular in space, the summation is in convolution form and can be accelerated by use of a FFT. In the electrostatic electromechanical switches, there are multiple conductors with air-gap or dielectrics, which form a capacitance matrix. A conductor in CoventorWare is analogous to a circuit node. In MemElectro, the user sets all the conductors to particular voltages, and the net charge on each conductor is then computed. The nodal capacitance matrix provides the relationship between charge and voltage. Figure 6.2 shows how the nodal capacitance matrix corresponds to the circuit network. The capacitance matrix of the figure also illustrates that the off-diagonal terms of the capacitance matrix correspond directly to the circuit capacitance values. The capacitance matrix possesses several properties such that all elements on the main diagonal are positive and the rest of the elements are negative. Also, it is symmetric, i.e. $C_{ij} = C_{ji}$ and the sum of all elements in every column and every row is equal to zero, which is a result of charge conservation. The capacitance matrix, then, relates the net charge on a conductor in the problem to any applied voltage offset to the zero reference by computing the product of capacitance and potential matrices [322]. For problems with conductors and dielectrics, the force on the dielectric may also be calculated from a work/energy point of view. The energy in the components is given an applied voltage difference ΔV with a capacitance, C, and its electrostatic force can be calculated as discussed in Chapter 2.

6.2.2. MemMech

6.2.2.1. Static Analysis

The MemMech is a solver based on the FEM method. To understand it operation we need to have a good understanding of FEM for static analysis. As an example, Figure 6.3 shows a truss, constrained at one end and loaded at the other end. The objective of the analysis is to find the displacement of the free end of the truss, the stress in the truss, and the reaction force at the constrained end of the truss. The first step of any finite element simulation is to discretize the actual geometry of the structure using finite elements. Each finite element represents a discrete portion of the physical structure. The finite elements are joined by shared nodes. The nodes and finite elements make up the mesh. The number of elements used in a particular mesh is referred to as the mesh density. In CoventorWare, the mesh is specified and created in the Preprocessor. The user must carefully consider what type and density of mesh to create because in a stress analysis the displacements of the nodes are the fundamental variables that MemMech calculates.

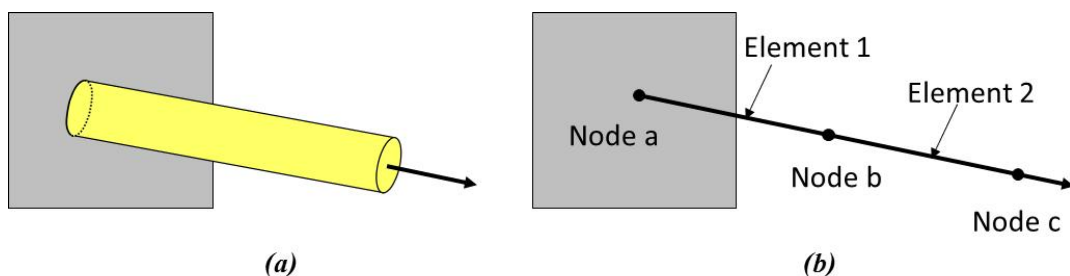


Figure 6.3: (a) A truss example, (b) Discretized truss model ; Reproduced from [321].

Once the nodal displacements are known, the stresses and strains in each finite element can be determined. The example in Figure 6.3 (a) will be modeled with two truss elements. Truss elements can carry axial loads only. The discretized model is shown in Figure 6.3 (b) and free-body diagrams for each node in the model are shown in Figure 6.4.

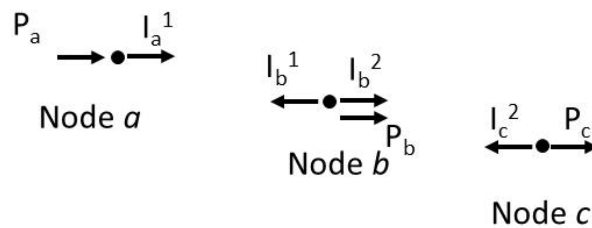


Figure 6.4: Free-Body Diagram of Truss Nodes; Reproduced from [321].

In general, each node carries an external load applied to the model, "P", and internal loads, "I", caused by stresses in the elements attached to that node. For a model to be in static equilibrium, the net force acting on each node must be zero. This means that the internal and external loads at each node must balance each other. For "Node *a*", this equilibrium equation can be obtained by assuming that the change in length of the rod is small and the strain in Element 1 is given by

$$\varepsilon_{11} = \frac{u^b - u^a}{L} \tag{6.2}$$

, where u^a and u^b are the displacements at Nodes a and b, respectively, and L is the original length of the element. Assuming that the material is elastic, the stress in the rod is calculated by multiplying the strain by the Young's modulus, *E*,

$$\sigma_{11} = E\varepsilon_{11} \tag{6.3}$$

The axial force acting on the end node is equivalent to the stress in the rod multiplied by its cross-sectional area, A. Thus, a relationship between internal force, material properties, and displacements can be obtained as below.

$$I_a^1 = \sigma_{11}A = E\varepsilon_{11}A = \frac{EA}{L}(u^b - u^a) \tag{6.4}$$

Then, in equilibrium, the net force at "Node a" can be written as

$$P_a + \frac{EA}{L}(u^b - u^a) = 0 \tag{6.5}$$

The net force equation at "Node b" should take into account the internal forces acting from both elements joined at that node because the internal force from "Element 1" is now acting in the opposite direction and becomes negative. The resulting equation is given by

$$P_b - \frac{EA}{L}(u^b - u^a) + \frac{EA}{L}(u^c - u^b) = 0 \tag{6.5}$$

Also, the net force equation at "Node c" is given by

$$P_c - \frac{EA}{L}(u^c - u^b) = 0 \tag{6.6}$$

To obtain the displacements of all the nodes, these equilibrium equations have to be solved simultaneously using matrix techniques. If the properties and dimensions of the two elements are the same, the equilibrium equations can be simplified as below.

$$\begin{Bmatrix} P_a \\ P_b \\ P_c \end{Bmatrix} - \left(\frac{EA}{L}\right)\begin{bmatrix} 1 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 1 \end{bmatrix}\begin{Bmatrix} u^a \\ u^b \\ u^c \end{Bmatrix} = 0 \tag{6.7}$$

Generally, the element stiffness, the EA/L terms, may be different from element to element. Therefore, we could rewrite the element stiffness as K_1 and K_2 for the two

elements in the model as below.

$$\begin{Bmatrix} P_a \\ P_b \\ P_c \end{Bmatrix} - \begin{bmatrix} K_1 & -K_1 & 0 \\ -K_1 & (K_1 + K_2) & -K_2 \\ 0 & -K_2 & K_2 \end{bmatrix} \begin{Bmatrix} u^a \\ u^b \\ u^c \end{Bmatrix} = 0 \qquad (6.8)$$

This system of equations can be solved to obtain values for the three unknown variables such as u^b, $u^c$and P_a because u^a is specified as 0.0. Once the displacements are known, we can calculate the stresses in the truss element.

6.2.2.2. Dynamic analysis

A static analysis is sufficient if the user is interested in the long-term response of a structure to applied loads. However, if the duration of the applied load is short, or if the loading is dynamic in nature, the user must perform a dynamic analysis. A dynamic simulation is one in which inertial forces are included in the dynamic equation of equilibrium and it is called as Euler-Bernoulli beam equation given by Equation 2.40. For simplicity, it can be rewritten as below,

$$m\ddot{u} + I - P = 0 \qquad (6.9)$$

where m is the mass of the structure, $\ddot{u}$ is the acceleration of the structure, I is the internal force in the structure and P is the applied external force.

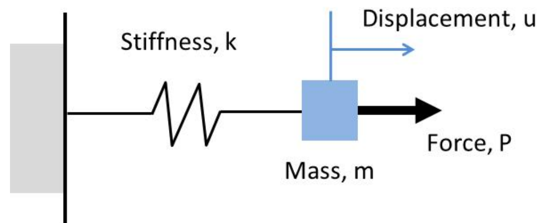


Figure 6.5: A mass-spring system; Reproduced from [321].

The inclusion of the inertial forces $(m\ddot{u})$ in the equation of equilibrium is the major difference between static and dynamic analyses. Another difference between the two types of simulations is in the definition of the internal forces (*I*). In a static analysis, the internal forces arise only from the deformation of the structure. However, in a dynamic analysis, the internal forces contain contributions created by both the motion (i.e., damping) and the deformation of the structure. The simplest dynamic problem is that of a mass oscillating on a spring, as shown in Figure 6.5. In this system, the internal force in the spring is given by ku, therefore, its dynamic equation of motion is given by

$$m\ddot{u} + ku - P = 0 \tag{6.10}$$

This mass-spring system has a natural frequency given by

$$\omega = \sqrt{\frac{k}{m}} \tag{6.11}$$

If the mass is moved and then released, it will oscillate at this frequency. If the force is applied at this frequency, the amplitude of the displacement will increase dramatically. This phenomenon is known as resonance. Real structures have a large number of natural resonant frequencies, which can be determined by considering the dynamic response of the unloaded structure (P=0) as discussed in Chapter 2. The frequency extraction procedure in MemMech is used to determine the modes and corresponding resonant frequencies of the structure. This procedure is easy to use in that the user needs only specify the number of modes required or the maximum frequency of interest.

6.2.3. CoSolveEM

CoSolveEM provides the capability of coupled quasi-steady electromechanical analysis. A typical application is the analysis of the electrostatic actuation of restrained mechanical structures. As reviewed, MemElectro provides the electrostatic analysis, and MemMech provides the mechanical analysis. CoSolveEM uses an iterative procedure to maintain consistency between the two solutions, that is, the mechanical deformation is correct for the applied electrostatic forcing. For example, when a voltage is applied between two conductors in a MEMS switch, it generates an attractive electrostatic force between the two conductors. This force will result in the mechanical deformation of the structure. A critical aspect of this behavior is that the deformation will reduce the distance between the two conductors. As a result, the restoring force for the structure will increase linearly with some measure of the deflection of the structure, while the electrostatic force will increase inversely with the square of the distance between the conductors. It is this force relationship that leads to the phenomenon of pull-in. Pull-in refers to the fact that for two suspended conductors, a trajectory of increasing voltage bias will increasingly deform the structure to a point where the deformation will become unstable, and deformation will increase without bias increase to the point of contact between the conductors. Determining the pull-in voltage for a device consists of finding the greatest voltage bias that can be supported before pull-in occurs. This means numerically determining a weakly stable state. In an iterative procedure to find such a state, convergence can be difficult to achieve. On the lower voltage side of this state, convergence is not difficult. While on the higher side, the procedure will diverge. The

CoSolveEM module will modify the voltage trajectory to find the pull-in voltage bias. Given a user-defined trajectory that begins at a low voltage and consistently increments that voltage to a point beyond the pull-in voltage bias, CoSolveEM will determine the voltage at which the iterative procedure between the electrostatic forcing and the mechanical restoring diverges and will systematically reduce the voltage step so as to determine the voltage bias range in which the consistency between the forcing and restoring becomes unstable.

In this simulation work, CoSolveEM was used to simulate the "pull-in voltage" and MemMech was used to simulate the "Mechanical Resonant Frequency" for each MEMS switch structure.

6.2.4. Limitations

There are several limitations in the CoventorWare simulation. First, the single-walled carbon nanotube is not provided in the default materials data base, but CoventorWare allows adding a material into the data base. We assumed a mass density of 1.4g/cm^3 and took the Young's modulus as the minimum value from AFM and tribonanoindentation tests (350GPa).

	Beam		***Gate1***	***Gate2***	***Drain***	***Spacing***
	Length	***Width***	***Width***	***Width***	***Width***	
A	***14.0μm***	***2.0μm***	***2.0μm***	***2.0μm***	***2.0μm***	***2.0μm***
B	***7.0μm***	***1.0μm***	***1.0μm***	***1.0μm***	***1.0μm***	***1.0μm***
C	***4.2μm***	***0.6μm***	***0.6μm***	***0.6μm***	***0.6μm***	***0.6μm***

Table 6.1: Basic simulation structures specification designed in the CoventorWare.

Furthermore, the SWNT beam should be flat in order for the simulation to be well converged so curvature and film roughness could not be considered. Third, small devices were simulated by scaling down a basic structure due to an undiagnosed divergence issue that appears to be inherent to the code or mesh generation. As a result, very small devices could not be simulated. The width (W) and length (L) of SWNT beam in the basic structure are 2μm and 14μm, respectively. (The width of electrodes and the spacing between electrodes are all 2μm.) In this work, the used scaling factors were 1, 0.5 and 0.3, which produced 3 different sizes of SWNT beams, W/L=2μm/14μm, 1μm/7μm, and 0.6μm/4.2μm as listed in the Table 6.1.

6.3. Simulated Basic Device Structure

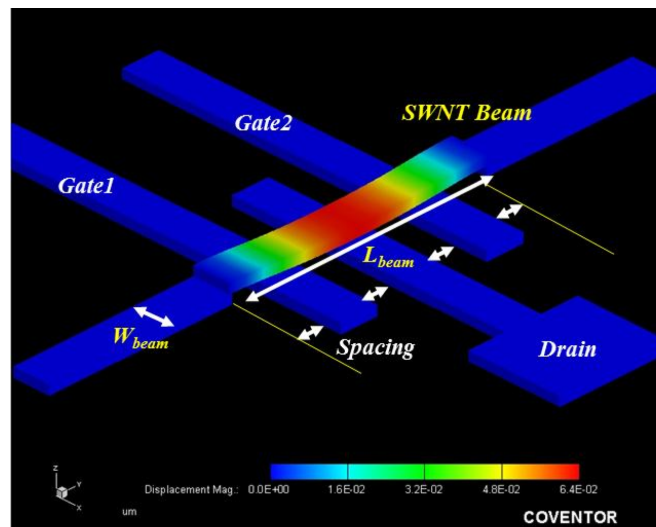


Figure 6.6: Basic simulation structure designed in the CoventorWare.

The basic simulation structure of 3-terminal MEMS switch is shown in the Figure 6.6. When a bias is forced between a movable beam and the gates, the electrostatic force pulls on the beam, deflecting it down against the elastic restoring force. To simulate this switching operation, especially the "pull-in" event, both elastic restoring and electrostatic forces must be considered. The CoventorWare provides the coupled electromechanical simulation module to detect the "pull-in" of a simulated MEMS device using the "detect pull-in" option of "CosolveEM" module. The fundamental resonant frequency was obtained by forcing a load at the center of a beam in the CoventorWare simulation using the modal analysis of "MemMech" module.

6.4. Biasing Condition Dependency for Actuation

A 3-terminal MEMS switch consists of several capacitors such as C_{sg1}, C_{sg2}, C_{sd}, and fringing capacitances between electrodes as described in the Figure 2.5. The fringing capacitances could be negligible due to the thick oxide between electrodes. However, the C_{sg1}, C_{sg2} and C_{sd} would play a critical role in the device operation. In this section, their effects are discussed in terms of how the pull-in voltage depends on which electrode(s) is biased.

6.4.1. Drain Biasing vs. Gate Biasing vs. Beam Biasing

When two gates are biased and others are grounded, electric charges are mainly stored in the capacitances C_{sg1} and C_{sg2}. For drain biasing, charge would be mainly stored

in the C_{sd}. Similarly, in case of beam biasing, charge would be stored in C_{sg1}, C_{sg2}, and C_{sd}. In addition, the spring constant would be different. For drain bias, the beam is likely to be loaded at the center and it could be modeled as Equation 2.7. In case of gate bias, the beam is likely to be loaded off-center and could be modeled as Equation 2.12. And in case of beam biasing, the beam is likely to be loaded uniformly all over it. From Equation 2.6, its spring constant could be modeled as [20]

$$k_{stiffness} = 32Ew\left(\frac{t}{l}\right)^3, \tag{6.12}$$

Therefore, in terms of effectiveness for capacitance and mechanical response,

(1) $Total\ Capacitance : (Beam\ biasing) \gg (Gate\ biasing) > (Drain\ biasing)$

(2) $Spring\ Constant : (Gate\ biasing) \gg (Beam\ biasing) > (Drain\ biasing)$

From this perspective, we could expect the pull-in voltage in case of beam biasing would be smaller than others. The simulation results are consistent with this view as shown in Figure 6.7.

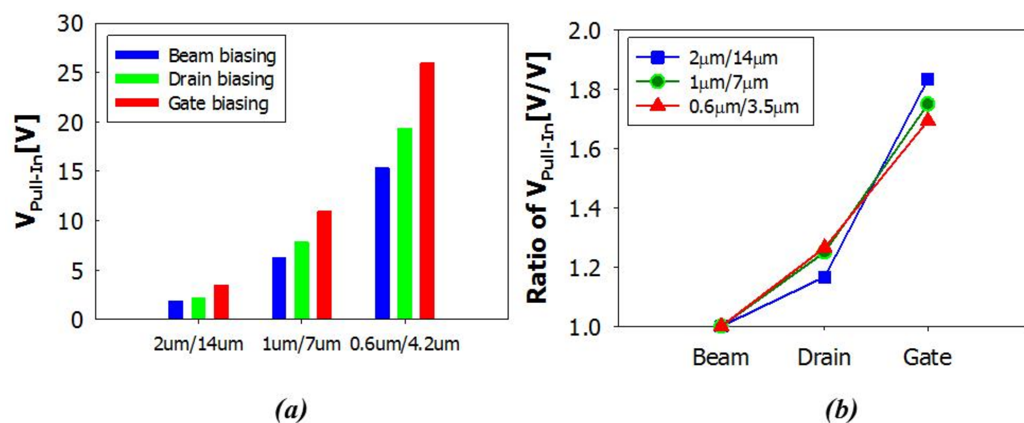


Figure 6.7: Actuating electrode dependency on Pull-in voltage; (a) Simulated pull-in voltages, (b) ratio of pull-in voltages referenced by beam biasing.

As expected, the pull-in voltage was the lowest when it was actuated with the beam electrode. It was the highest when it was actuated with the two gate electrodes. However, as the device becomes smaller, Figure 6.7(b) shows an opposite tendency in the pull-in voltage. In comparison "Beam biasing" with "Drain biasing", the changes of pull-in voltages in smaller devices than 2μm/14μm tend to be relatively larger.

6.4.2. Single-Gate Biasing vs. Dual-Gate Biasing

The capacitance of single-gate biasing would be half of dual-gate biasing, which would result in an increase of pull-in voltage with ratio of $\sqrt{2}$, equivalently about 40%, due to the relationship between capacitance and pull-in voltage from equation 2.22 through 2.28. Therefore, the pull-in voltage of single-gate biasing would be bigger than the dual-gate biasing. The simulation result shows that the pull-in voltage of single-gate biasing is about 20% bigger than the dual-gate biasing, as shown in Figure 6.8.

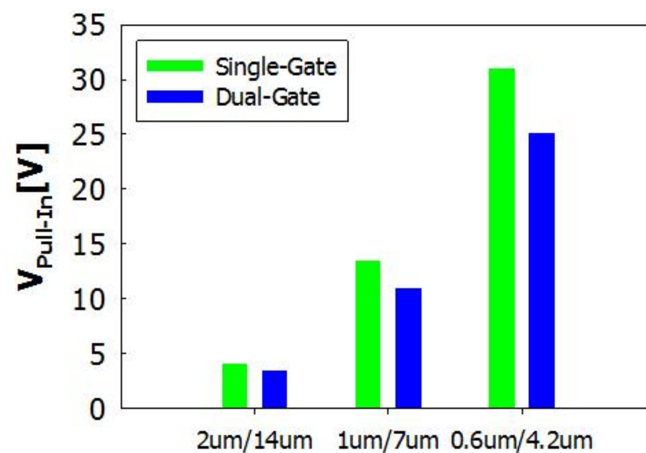


Figure 6.8: Pull-in voltage dependency on single gate biasing vs. dual gate biasing.

6.5. Geometry Effects on 3-Terminal Fixed-Fixed MEMS Switch

As reviewed in chapter 2, the pull-in voltage and mechanical resonant frequency of a 3-terminal fixed-fixed MEMS switch are intrinsically dependent on the dimensions and mechanical properties of a suspended beam and air-gap [20, 64]. In this section, the fundamental process dependencies of a 3-terminal electrostatic MEMS switch are discussed using the CoventorWare simulation results. Also, the simulation data will be compared with the closed-form models of pull-in voltage and fundamental resonant frequency.

6.5.1. Free-Standing Film Thickness Dependency

Four different beam thicknesses of 50, 100, 150 and 200nm were simulated for W/L=2μm/14μm, 1μm/7μm and 0.6μm/4.2μm with a 50nm of air-gap as shown in Figure 6.9. The simulated pull-in voltage and fundamental resonant frequency were strongly dependent on the beam thickness. From the spring constant equation 2.12 and pull-in voltage model equation 2.28, the pull-in voltage is proportional to $(beam\ thickness = T)^{1.5}$. Also, from the fundamental resonant frequency model equation 2.53, it is linearly proportional to the beam thickness.

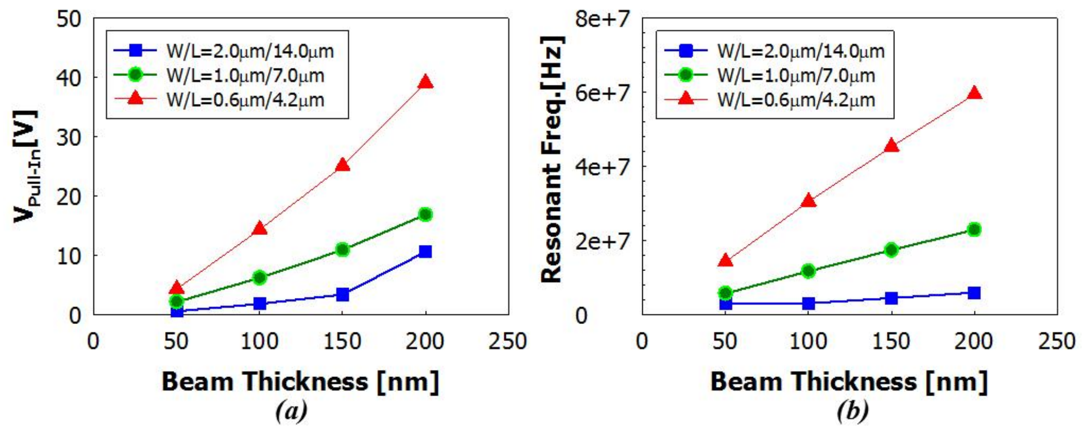


Figure 6.9: The beam thickness dependency from CoventorWare simulation in terms of (a) pull-in voltage, and (b) fundamental resonant frequency.

In addition, the simulation data were compared with the closed form models for pull-in voltage and fundamental resonant frequency, as shown in Figure 6.10. A fit of the CoventorWare simulation data shows a dependence of $T^{1.47\sim1.57}$ for pull-in voltage and $T^{0.95\sim1.03}$ for fundamental resonant frequency depending on device sizes, consistent with the theoretical dependence except for abnormal data at W/L=2µm/14µm (open-square in the Figure 6.10 (e) and (f)).

This could be understood considering the spring constant and resonant frequency dependency on the beam thickness. The spring constant of a fixed-fixed beam is proportional to the cubic square of the beam thickness and its mechanical resonant frequency is linearly proportional to the beam thickness as introduced in Chapter 2.

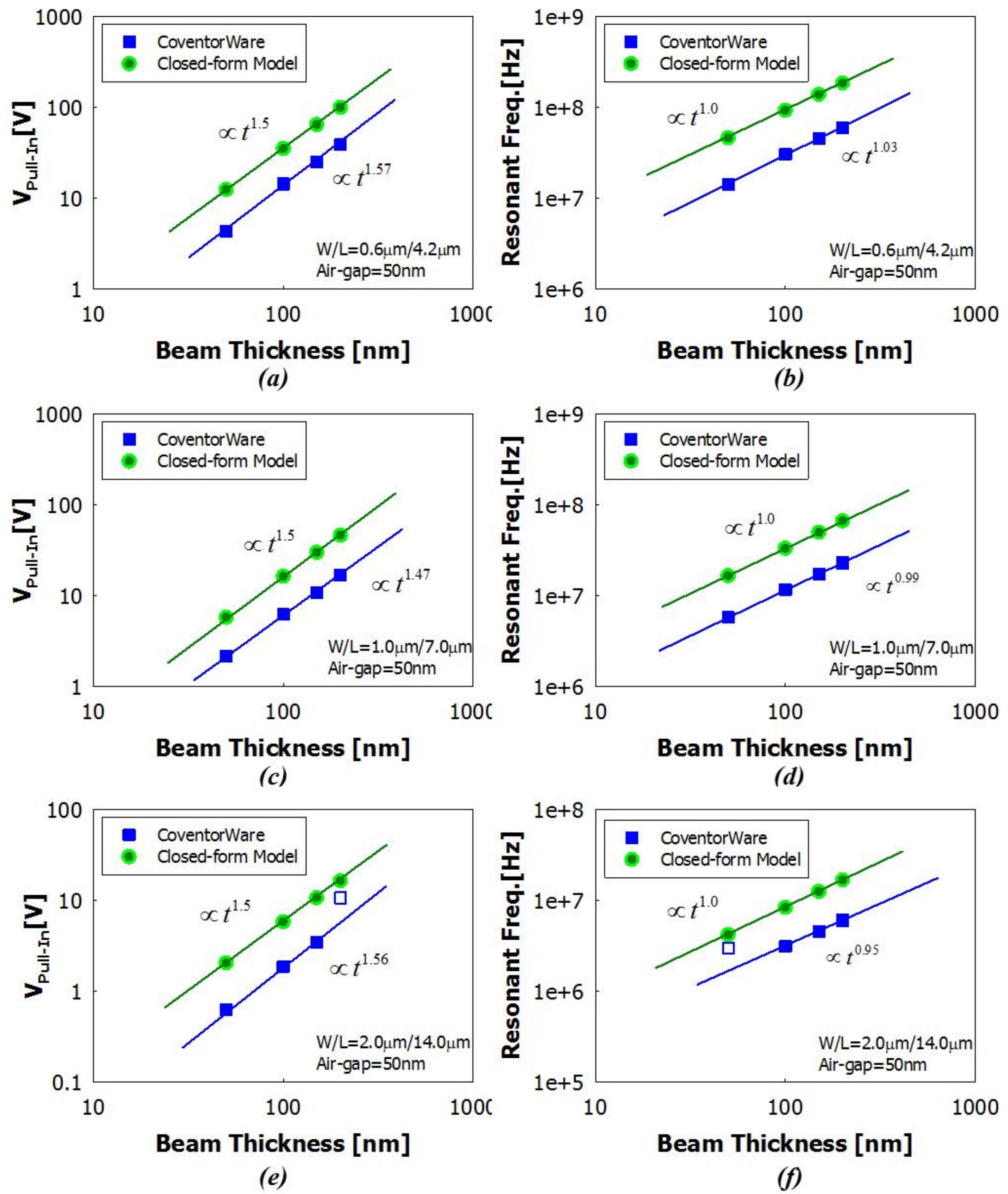


Figure 6.10: The beam thickness dependency comparison with CoventorWare simulation data and closed form models in terms of pull-in voltage (a, c, e), and fundamental resonant frequency (b, d, f) for different device sizes.

6.5.2. Free-Standing Film Width Dependency

The film width contributes to the spring constant of a fixed-fixed beam as seen in Equation 2.12. However, it is cancelled out in the pull-in voltage model in Equation 2.28 and there is no relationship to the mechanical resonant frequency as in Equation 2.53. For a device with W/L=2µm/14µm, three different beam widths, 1µm, 2µm and 4µm, were simulated with a 50nm of air-gap and a 100nm thick beam. Moreover, for further simulations, these devices were scaled with the ratio of 0.5 and 0.3. The simulation results are also consistent with this model as shown in Figure 6.11.

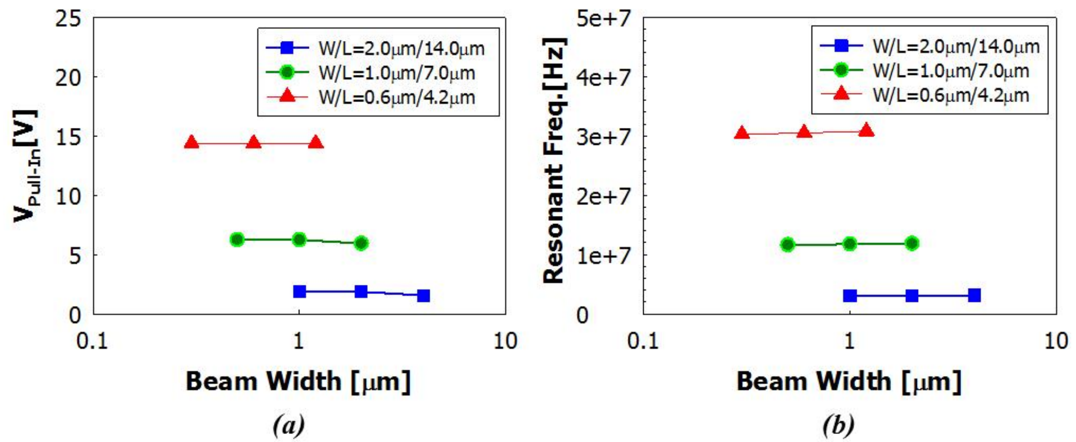


Figure 6.11: The beam width dependency from CoventorWare simulation in terms of (a) pull-in voltage, and (b) fundamental resonant frequency.

6.5.3. Air-gap Dependence

The simulated air-gaps were 20nm, 50nm and 100nm with a 100nm thick beam and Figure 6.12 shows the simulation results. From Equations 2.20 and 2.28, the pull-in voltage is proportional to $(air - gap = g_{air})^{1.5}$, but there is no direct relationship with fundamental resonant frequency as described in Equation 2.53. The pull-in voltage simulation results were proportional to $(g_{air})^{1.09\sim1.29}$depending on the device sizes and the pull-in voltage dependency on g_{air} tends to be slightly decreased at small devices, as shown in Figure 6.13.

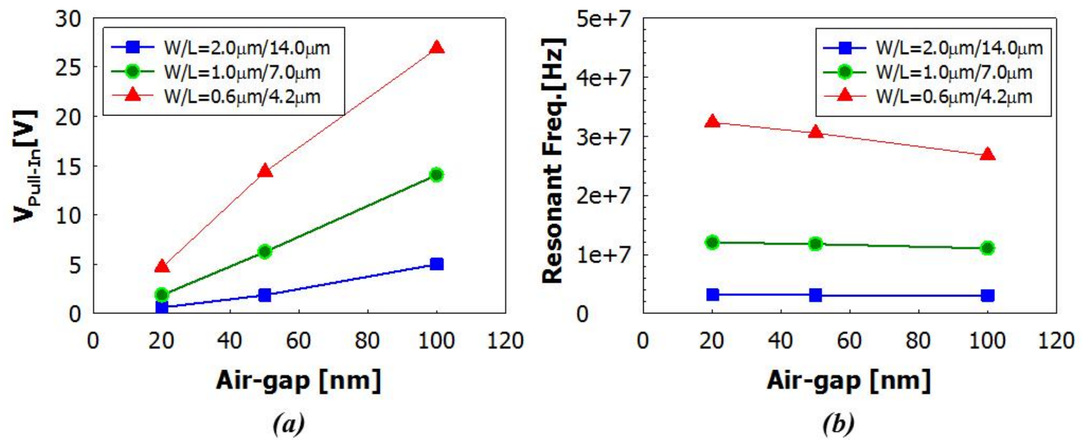


Figure 6.12: The air-gap dependency from CoventorWare simulation in terms of (a) pull-in voltage, and (b) fundamental resonant frequency.

The fundamental resonant frequency simulation data tends to be slightly decreased when the air-gap is increased, even though there is no relationship with the air-gap in the closed-form model. Especially, for a device of W/L=0.6μm/4.2μm, the fundamental

resonant frequency tends to be decreased with a ratio of $(g_{air})^{-0.12}$ with increasing air-gap. This might be due to an increase of the effective beam length for a larger air-gap at the anchor. Although the change was very small, the W/L=1μm/7μm device shows a similar tendency.

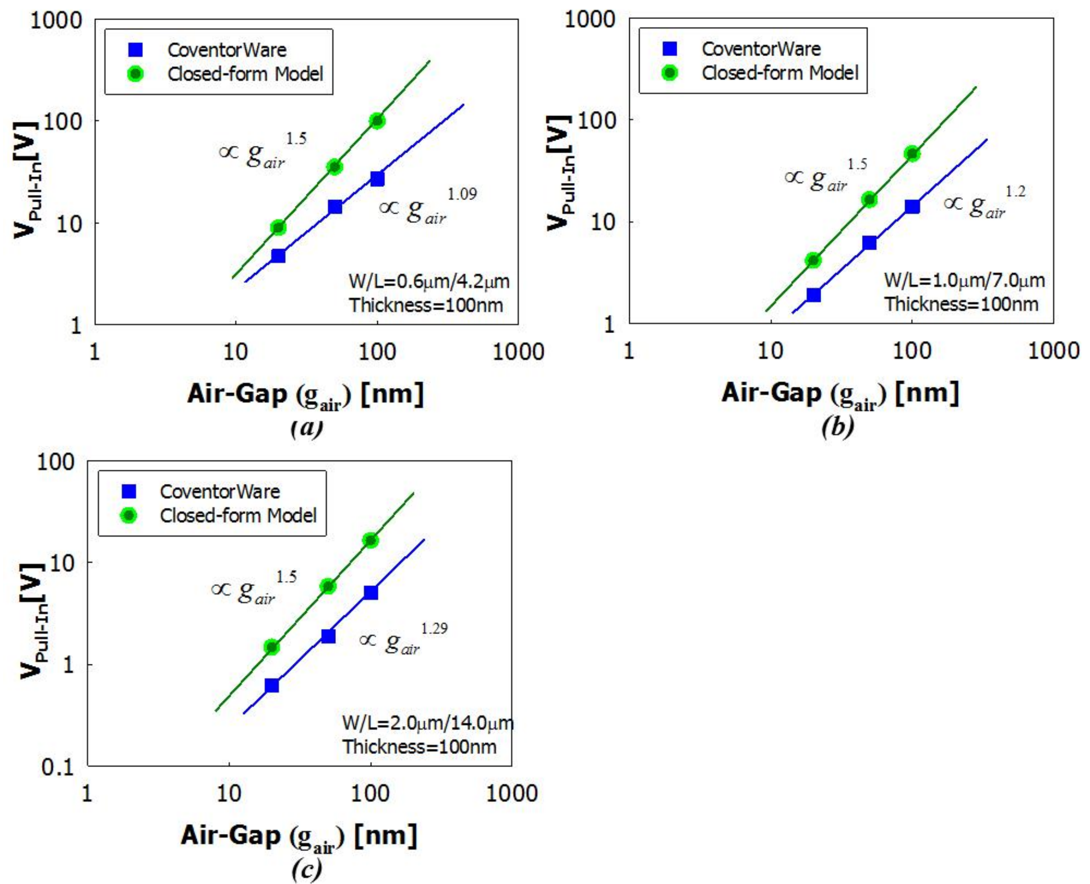


Figure 6.13: The air-gap dependency comparison with CoventorWare simulation data and closed form model in terms of pull-in voltage with E=350GPa in cases of (a) W/L=0.6μm/4.2μm, (b) W/L=1.0μm/7.0μm, and (c) W/L=2.0μm/14.0μm.

6.5.4. Beam Length Dependency

From the closed-form models of the pull-in voltage and fundamental resonant frequency, the former is proportional to $(Beam\,length = L)^{-1.5}$ and the latter is proportional to $(Beam\,length = L)^{-2}$. Using the simulation results on the devices with 50nm of air-gap and 100nm of beam thickness, we could find a dependency in terms of beam length for pull-in voltage and fundamental resonant frequency. This is possible because we could ignore the beam width effect as discussed in 6.5.2. As shown in Figure 6.14, the simulated pull-in voltages are proportional to $L^{-1.69}$ and the simulated fundamental resonant frequencies are proportional to $L^{-1.9}$, which is almost same dependency as closed-form models for both pull-in voltage and fundamental resonant frequency.

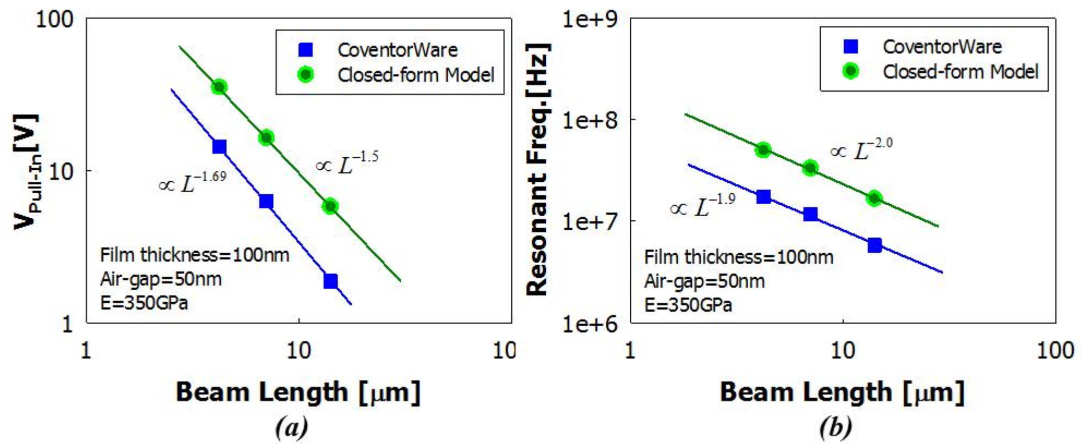


Figure 6.14: The beam length dependency comparison with CoventorWare simulation data and closed form model in terms of (a) pull-in voltage, and (b) fundamental resonant frequency.

6.5.5. Beam-Gate Overlap Area Dependency

As discussed in Section 6.4, the capacitance between a beam and the gate plays an important role in determining the pull-in voltage of an electrostatic MEMS switch.

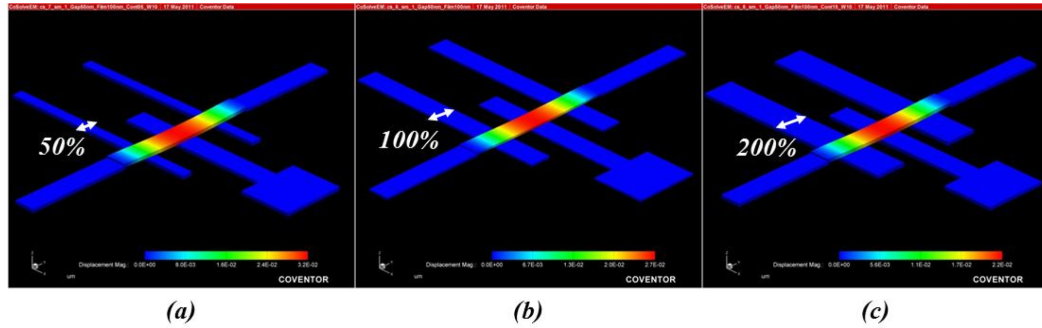


Figure 6.15: CoventorWare simulation structures for the gate electrode width dependency on pull-in voltage; (a) 50%, (b) 100%, (c) 200% of a reference.

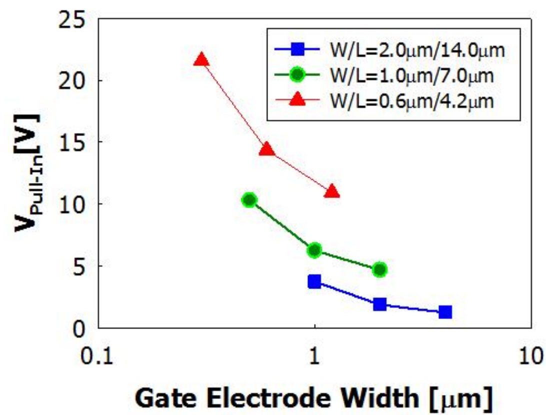


Figure 6.16: The gate electrode width dependency from CoventorWare simulation for pull-in voltage.

First, it was checked by changing the width of gate electrodes. Changes of -50% and +200% from the standard over the gate electrodes were used. The device considered

had a 50nm air-gap and a 100nm thick beam, as shown in Figure 6.15. In this case, the fundamental resonant frequency is not changed. The simulation results are shown in Figure 6.16. From this concept, we extended to the beam shape engineering, which was introduced to control the pull-in voltage without any changes in the process parameters. The basic idea is to increase or decrease the overlap area between gate electrodes and a free standing beam. This allows one to easily use multiple pull-in voltages in the same circuit without any additional process complexity.

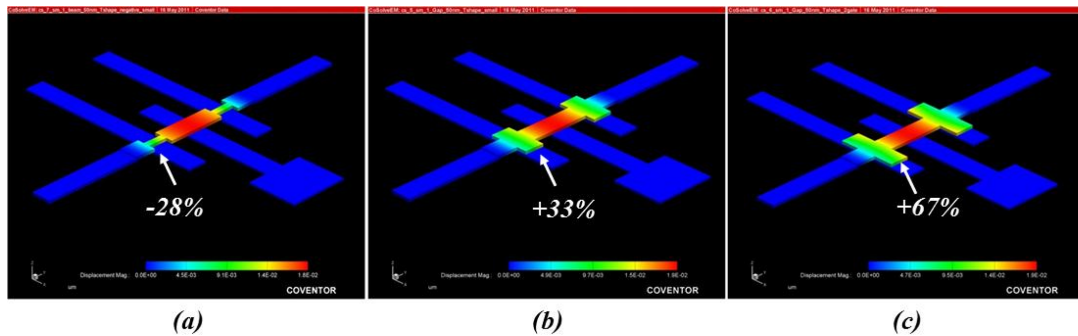


Figure 6.17: CoventorWare simulation structures to estimate the dependency on the extra overlap area between two gates and a beam by changing beam shapes.

Figure 6.17 depicts the designed simulation structures by modifying the beam shape. Depending on the beam shapes, the pull-in voltages and fundamental resonant frequencies were estimated as shown in Figure 6.18. The pull-in voltages could be lowered by 30% compared to a simple bar device when the overlap area between extra-gate and a beam overlap area is increased to 30% of total overlap area, as shown in Figure 6.18 (a) and (b).

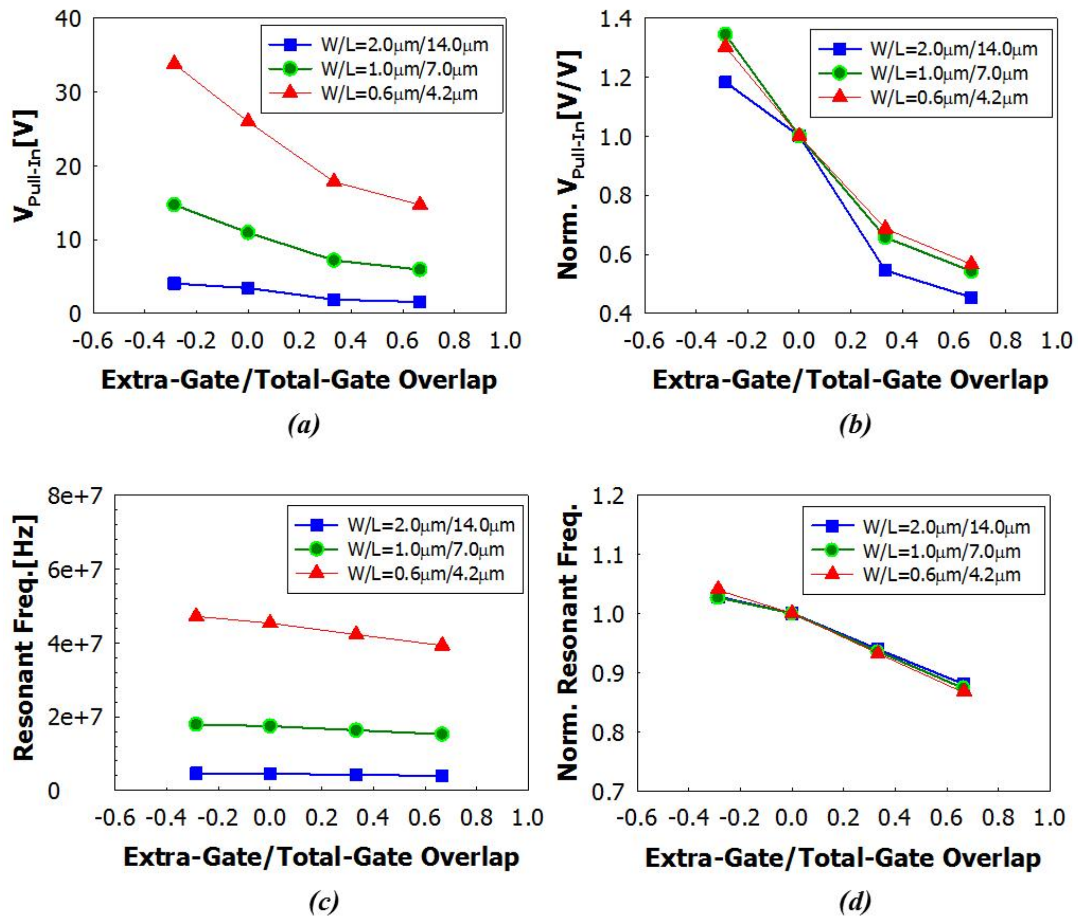


Figure 6.18: The extra-gate overlap area between two gates and a beam dependency from CoventorWare simulation: (a) simulated pull-in voltage, (b) normalized pull-in voltage, (c) fundamental resonant frequency, and (d) normalized fundamental resonant frequency.

However, when the extra overlap area is increased to 66%, the change of pull-in voltage becomes smaller than that of 33% because the extra-beam area structures also acts as parasitic cantilever structures. As long as the extra overlap area between two gates and a beam is controlled within ±30% of total overlap area, we could control the pull-in voltage of a device without changing its overall dimensions. In this approach, the beam

shape was engineered to control the pull-in voltage, which results in also changing the fundamental resonant frequency because its inertia should be changed depending on the beam shapes as shown in Figure 6.18 (c) and (d). However, the amount of frequency change is less than 10%, when the extra overlap area is changed to 30% of total overlap area.

6.6. Conclusions

In this section, the fundamental process dependencies of the electrostatic MEMS switches were estimated with CoventorWare simulations in terms of the pull-in voltage and the fundamental (1st mode) resonant frequency. The simulation results are mostly consistent with the closed form pull-in voltage and the 1st mode resonant frequency models. Moreover, it is believed that the pull-in voltage of an electrostatic MEMS switch could be controlled by changing the extra overlap area between two gates and a beam.

CHAPTER 7: CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1. Conclusions

Although the electrostatic MEMS/NEMS switch has an excellent standby leakage, it has not been a successful replacement of CMOS devices due to its large mechanical delay. Single-walled carbon nanotubes (SWNT) have very low mass density and strong mechanical properties. Using both device modeling and experiments, we demonstrated that the use of SWNT based thin films as a suspended beams for electrostatic MEMS/NEMS switch can be a route to low power and high switching speed which would move these devices off of the trend for pull-in voltage versus switching speed from literature

To provide better applicability, MEMS/NEMS switches should be able to be fabricated either before or after CMOS fabrication process. If the MEMS/NEMS switches are processed after CMOS fabrication, one of critical issues may be the process temperature during the carbon nanotube (CNT) film deposition. In addition, the selected CNT film deposition process should be applicable to various kinds of substrates. Chemical vapor deposition (CVD) is one of most popular thin film deposition process for carbon nanotubes and amorphous silicon, oxide, nitride and even metal deposition for the CMOS fabrication. However, it typically requires a high process temperature (>600˚C). Therefore, for this work, layer-by-layer (LbL) self-assembly and dielectrophoresis were

used for aligned-composite and pure SWNT thin film depositions for MEMS/NEMS switch application.

We fabricated 2-terminal fixed- beam switches with aligned composite SWNT thin films, which were prepared by dielectrophoretic process with LbL self-assembly. The dense membranes were successfully patterned to form submicron beams by e-beam lithography and oxygen plasma etching. Fixed-fixed beam switches using these membranes successfully operated with approximately 600 psec switching delay and as low as 3 V dc pull-in. From this experiment, we confirmed that the SWNT based thin film have the potential to make fast MEMS switches with a low operation voltage due to its low mass density and high stiffness.

However, the aligned-composite SWNT film uses copolymer stacks, which results in early device failure. Moreover, the dielectrophoretic deposition process is not applicable for complicated circuits and wafer-level applications because the two electrodes must be actively powered during the film deposition process for each device. We introduced a new SWNT deposition process to resolve these problems and still use the unique physical and electrical properties of SWNT. By replacing copolymer with positively functionalized SWNT, an all-SWNT film was deposited through LbL self-assembly without use of a copolymer, resulting in 75% reduction of resistivity compared to our previous composite film with copolymer, without the need for CNT alignment. The deposited film thickness is well controlled by changing the number of dipping cycles,

about 10nm per cycle. Moreover, we demonstrated that 3-terminal MEMS switch built with this all-SWNT thin film behaved like a NAND gate. Through thermal treatments, its on- and off-current ratio could be dramatically improved as well as the electrical properties of the all-SWNT film. However, thermal treatments caused an excessive reaction between gold electrodes and the amorphous silicon sacrificial layer due to the low eutectic temperature of the gold-silicon binary system. Furthermore, the extrinsic stress due to the plasma enhanced CVD (PECVD) SiO_2 and amorphous silicon layers caused a significant device yield drop. This could be improved by SiO_2 deposition on wafer backside. Therefore, this 3-terminal MEMS switch built with a pure SWNT film is believed to be a very promising device for low power digital logic applications, if its yield and reliability related issues should be resolved.

Furthermore, the fundamental process dependencies of the electrostatic MEMS switches were also estimated with CoventorWare simulations in terms of the pull-in voltage and the fundamental (1st mode) resonant frequency. The simulation results are mostly consistent with the closed form pull-in voltage and the 1st mode resonant frequency models. Moreover, it is shown that the pull-in voltage of an electrostatic MEMS switch could be controlled by changing the extra overlap area between two gates and a beam. This has the potential for significant impact in the design of digital logic using these devices.

7.2. Future Work

Our ultimate goal is to demonstrate a reliable logic operation with 3-terminal SWNT thin film based MEMS/NEMS switches. However, we encountered many obstacles such as early failure due to moisture absorption during test in the air, unwanted agglomerates/wrinkles during deposition process, an excessive reaction between gold and amorphous silicon, and extrinsic film stress effect. Therefore, further work on this project should be focused on improving their yield and reliability.

First, the released device after sacrificial layer removed as the last process should be stored in the vacuum or in the N_2 (nitrogen) filled globe box to minimize moisture absorption from the air. (In our work, most free standing beams were collapsed within two days when they were stored in the air.)

Second, the frequent sonication and centrifugation should be performed prior to and during film deposition process to minimize the CNT agglomerates which form due to the attractive van der Waals force between the CNTs. Moreover, a careful rinse and perfectly drying of sample wafer prior to each dipping step is required. When some agglomerates are formed in one or both of functionalized CNT dispersions, the deposited CNT film uniformity and especially, surface roughness become substantially worse, resulting in unexpected device failure and/or performance degradation.

Third, a new metal for fixed electrodes instead of gold should be considered to prevent the excessive reaction with amorphous silicon during thermal treatment due to their low eutectic temperature. Good candidates are platinum and palladium, which have higher eutectic temperature. Additionally, due to their high work function, they have been

shown to make better ohmic contact with CNTs than gold.

Fourth, searching for a new sacrificial layer with low stress would be required instead of the current PECVD amorphous silicon process. A replacement sacrificial layer should be removable by dry etching to minimize the stiction problem during device release process. This could involve simply changing the deposition process. Porous silicon nitride deposited by PECVD at low temperature (50~100˚C) might also be a good candidate. Its stress is very low and, when measurable, tensile. It can be etched with an SF_6 plasma, although its etching speed would be slower than amorphous silicon. However, it could resolve the stress induced beam collapse issue.

Fifth, a new approach for the SWNT film deposition is required for better throughput than LbL self-assembly. As discussed in the chapter 4 and 5, it takes at least 15 to 30 minutes for each dipping cycle including rinse and dry for SWNT film deposition. To deposit a 100nm thick pure SWNT thin film, approximately 10 dipping cycles should be performed, which would result in 5 hours for film deposition process. Longer deposition process increase a possibility of forming agglomerates in each functionalized SWNT dispersion. As reviewed in the chapter 3, electrophoretic deposition is a good candidate. However, it requires a conductive seed layer for CNT deposition on the substrate, which could be an obstacle in the device release process. Therefore, it is believed that a deliberate study to resolve this limitation should be followed.

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