

**REALIZING ANALOG CIRCUITS IN DIGITAL
PROCESSES**

A DISSERTATION

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Dedication

To the memory of my beloved grandmom

Ammajamma

REALIZING ANALOG CIRCUITS IN DIGITAL PROCESSES

by Shubha Bommalingaihnappallya

ABSTRACT

While the CMOS processes move to the nanometer regime and become more “digital” in nature, the consumer demands continue to focus on power-efficiency and reconfigurability. The optimal solution no longer lies only in the circuit design space. One has to consider architecture changes and look at the system as a whole. This thesis presents four such case studies.

The multi-rate $\Sigma - \Delta$ ADC proposed in this thesis, is at its heart a multi-stage traditional $\Sigma - \Delta$ ADC where the first stage is running at ‘N’ times the sampling frequency. As ‘N’ tends to infinity, this approaches a hybrid $\Sigma - \Delta$ with a continuous-time(CT) front-end(FE). Thus, the new architecture exploits the best of both worlds - discrete and continuous. It has the clock-rate to power trade-off advantage of a discrete-time(DT) $\Sigma - \Delta$. It also has anti-aliasing feature similar to the continuous-time(CT) $\Sigma - \Delta$ without its sensitivity to clock-jitter and EMI.

In a similar architectural optimization, the position of the zeros of the noise transfer function (NTF) of a traditional $\Sigma - \Delta$ converter is altered by modifying the loop filter to create an N-Tone $\Sigma - \Delta$ converter. If the signals are then placed only in these noise valleys - a MC-OFDM, for example - a high signal-to-noise Ratio (SNR) can be

achieved. In its most simplest form - the number of noise valleys being one - the N-Tone $\Sigma - \Delta$ converter reduces to the familiar band-pass $\Sigma - \Delta$ converter.

A low-power three-lane $2^{31} - 1$ pseudo-random binary sequence (PRBS) generator is realized by multiplexing four appropriately delayed parallel sub-sequences running at one-fourth the data rate. The prototype achieves its low-power by amortizing the power of the PRBS core over the three lanes and by carefully partitioning out the overall architecture into CMOS and CML circuit spaces.

Finally, a cost-effective low-jitter clock-distribution in a noisy environment is realized by making use of the well-known T-line clock distribution schemes on-die and moving the power distribution for the clock-network into the package.

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Chapter 1

Introduction

While battery-life and versatility have been the basis of consumer trends; reduction in feature size has been the basis of CMOS process trends. Driven basically by the digital industry for faster processors, smaller devices in CMOS processes help realize high-speed chips. In conjunction with the reducing device size, the operating power supplies are also being lowered, in an attempt to avoid reliability issues and pushing the power envelope. The classical Dennard MOSFET scaling, where the device dimensions (t_{ox}, L, W) and supplies scaled by a factor of $1/kappa$ and the doping concentrations scaled by factor of $kappa$, ended at the $130nm$ node. Scaling stopped driving performance, materials took on the onus [2]. It was “strained-silicon” that provided the increased drives in the $90nm$ node [3]. And, the high-K metal gate transistors restored the gate oxide scaling at the $45nm$ node [4]. This aggressive CMOS device scaling has driven remarkable increase of the cut-off frequency well into the multi-GHz range. The f_T has increased

to $160GHz$ and above in the $65nm$ node [5]. Newer $40nm$ process nodes boast of an f_T of $200GHz$ [6].

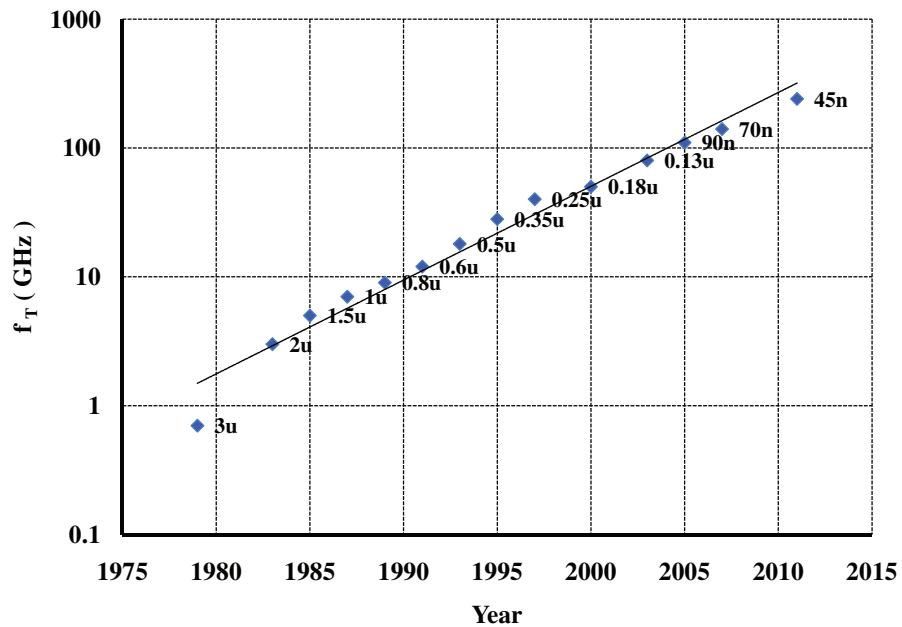


Figure 1.1: f_T trend for various CMOS process nodes

In fact, a very crude approximation of f_T is given by [7]. Figure 1.1 shows the f_T trend of the CMOS processes [8], [7], [9].

$$f_T = 10THz - nm/L_{min} \quad (1.1)$$

This increase in speed of digital devices hasn't come free. It has come only at the cost of increased leakages, increased device variations, reduced device matching - parameters that analog designers concern themselves with.

As device dimensions scale from one process node to another and oxide thickness

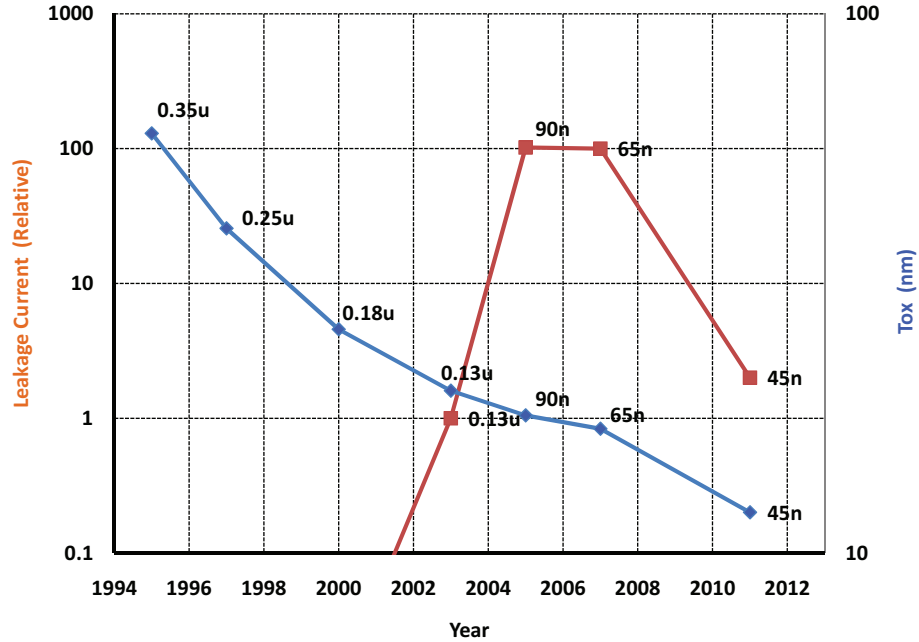


Figure 1.2: Gate-leakage trend for various CMOS process nodes

scales, the gate leakage also increases as tunneling becomes more dominant. The high-k Metal gate of 45nm enables 0.7X scaling of T_{ox} while also reducing the gate leakage by about 25X. Though this a favorable trend, compared to the sub-micron analog processes, the sub-nano digital processes still have higher leakages as shown in Figure 1.2 [10].

Device variation has two components to it - systematic variation and random variation. The systematic variation has remained comparable from process to process and is backed by the consistent yield numbers in the higher 90s (Figure 1.3). However, the random variation saw a steady increase right up till the 45nm node, pretty much like the gate leakage. With the advent of the high-k metal gate transistors, a significant dip in random variation was observed. However, further scaling of high-k metal transistors

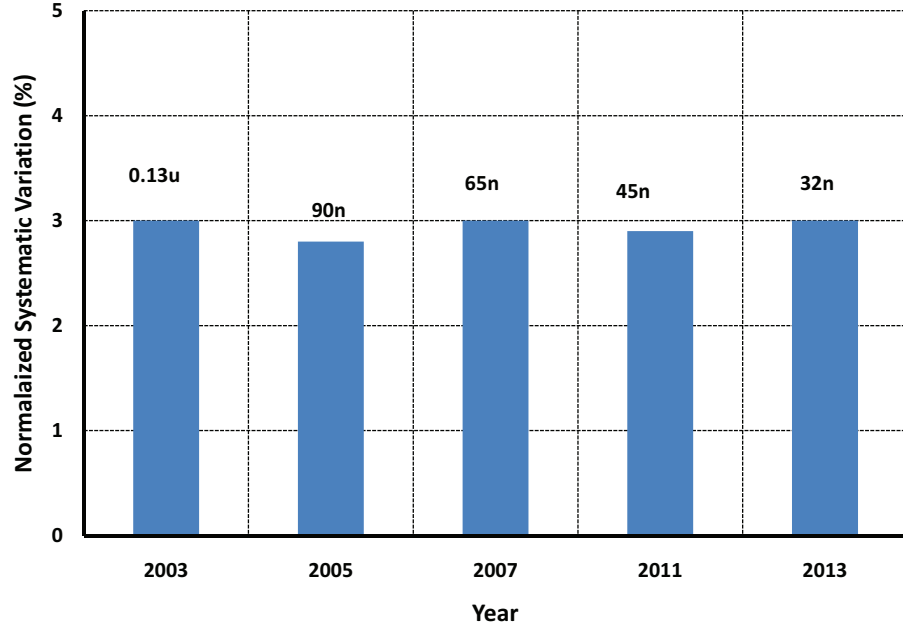


Figure 1.3: Systematic-variation trend for various CMOS process nodes

puts this random variation on an upward trend again as shown in Figure 1.4.

Figure 1.5 shows the C_{VT} trend of the processes [11]. C_{VT} is slope of the σVT versus $\frac{1}{\sqrt{L_{eff} \cdot W_{eff}}}$. It is frequently described by [12].

$$\begin{aligned}
 \sigma VT &= (4Nq^3\epsilon_{Si}\phi_B)^{1/4} \cdot \left(\frac{T_{ox}}{2\epsilon_{ox}}\right) \cdot \left(\frac{1}{\sqrt{L_{eff} \cdot W_{eff}}}\right) \\
 &= \frac{C_{VT}}{\sqrt{L_{eff} \cdot W_{eff}}}
 \end{aligned} \tag{1.2}$$

It is obvious that as feature size reduces, traditional analog methods cannot be employed due to the stringent matching and power implications.

Today, the wireless electronics industry is rampant with a number of technologies

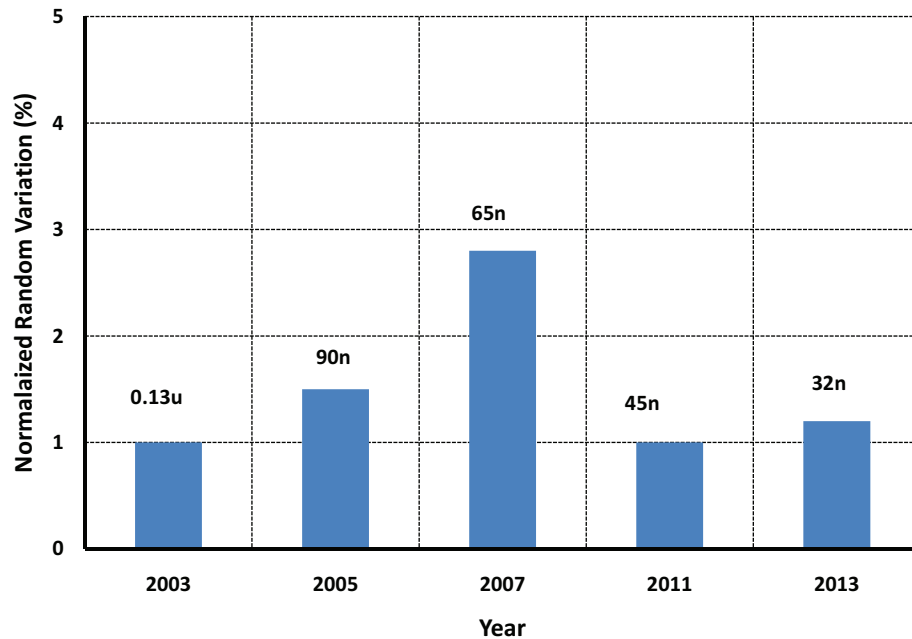


Figure 1.4: Random-variation trend for various CMOS process nodes

- GSM, EDGE, WCDMA, WLAN, Blue-tooth and UWB, to name a few. Each standard is optimized to cater to a specific set of users with different bandwidths, carrier-frequencies, and modulation schemes. The industry has been in the constant lookout for the ultimate solution - Software Defined Radio (SDR). To realize a power-optimal transceiver design, most of the processing should be done in the digital domain, mandating a conversion of the real-world analog signal to its discrete counterpart as early in the receiver chain as possible. The challenge then lies in faithfully encoding the analog signal in the presence of all the interferers without overloading the Analog-to-Digital Converter (ADC), while simultaneously maintaining a low power consumption and not compromising on reconfigurability.

When it comes to ADC design, $\Sigma\Delta$ architecture proves to be the architecture of choice for the afore-mentioned digital CMOS processes with increasing speed and device variations. It lends itself favorably by trading off speed for voltage-resolution[13]. Thus, the architecture works with the process and not against it. Study of prior research [14] shows that $\Sigma\Delta$ ADCs have been used to support multiple standards. Not only have the ADCs been optimized at a circuit-level to meet the specifications, but holistic approach of looking at the system as a whole has enabled making intelligent trade-offs to realize optimal system-levels solutions.

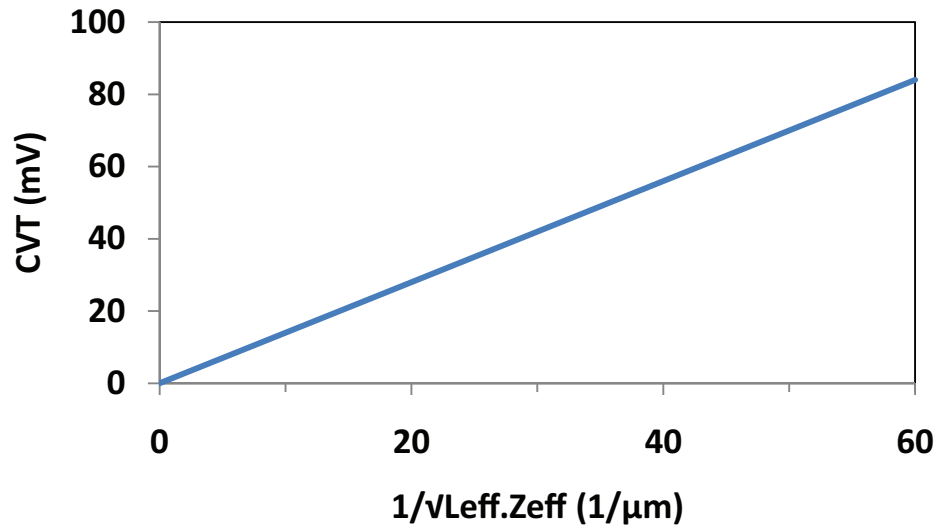


Figure 1.5: C_{VT} trend for various CMOS process nodes

Following the same trend of making system-level tradeoffs, Chapter 2 finds another way to relax the design requirements on the ADC. But before that, it briefly delves

into derivation of an ADC's dynamic range(DR) specifications. It proposes a new architecture where the first stage of a traditional two-stage $\Sigma\Delta$ ADCs now runs at a higher frequency, making use of the ever-increasing f_T of processes while allowing for the requirements on the dynamic-range to be reduced. This architecture along with the associated theory, behavioral model and circuits is presented as the "Multi-Rate $\Sigma\Delta$ ADC" in Chapter 2.

In Chapter 3, a quick look at the spectrum of the MC-OFDM UWB signal reveals a multi-tone nature. The "Multi-Tone ADC" presented in this chapter has a signal transfer function that perfectly complements the multi-tone signal. The chapter discusses the various possible modulator architectures for the multi-tone $\Sigma\Delta$ Converters and the performance of the ideal systems. It also presents the effect of circuit non-idealities on the performance of the converter by the simulation of its behavioral model and follows up with circuit implementations. It concludes with a multi-tone $\Sigma\Delta$ implementation in $130nm$ CMOS process.

Chapter 4 presents a novel way of designing a high-speed low-power multi-lane pseudo-random signal(PRBS) generator. Most suited for built-in test of multi-lane transceiver systems, due to the multiple PRBS streams available, the low-power aspect of the design is achieved by amortizing the power of the shared LFSR core over the multiple lanes. While these PRBS generators are used extensively in testing of transceiver channels, they can also be used for dithering in $\Sigma\Delta$ ADCs. This chapter presents the

thought process behind the architecture, the circuit implementation and the measurement results of a multi-lane PRBS generator prototype implemented in $130nm$ CMOS process. It also provides a comparison with other published designs.

Chapter 5 concludes with a look at how innovative ways can be used to realize a cost-effective and easy engineering solution to on-chip clock routing. It looks at existing solutions for low-jitter clock distribution and then describes a low-cost solution by taking advantage of the package.

Chapter 2

Multi-Rate $\Sigma - \Delta$ ADC

The multi-rate $\Sigma - \Delta$ ADC proposed in this chapter is at its heart a multi-stage traditional $\Sigma - \Delta$ ADC where the first stage is running at 'N' times the sampling frequency. As N tends to infinity, this approaches a hybrid $\Sigma - \Delta$ with a continuous-time(CT) front-end(FE). The Multi-rate ADC, thus exploits the best of both worlds - discrete and continuous. It has the clock-rate to power trade-off advantage of a discrete-time(DT) $\Sigma - \Delta$. It also has anti-aliasing feature similar to the continuous-time(CT) $\Sigma - \Delta$ without its sensitivity to clock-jitter and EMI. This chapter presents the multi-rate $\Sigma - \Delta$ modeled in SIMULINK. Spectre simulations in a 0.13 μ m process shows about 25dB suppression of the image which is at 5X the signal frequency.

2.1 Motivation

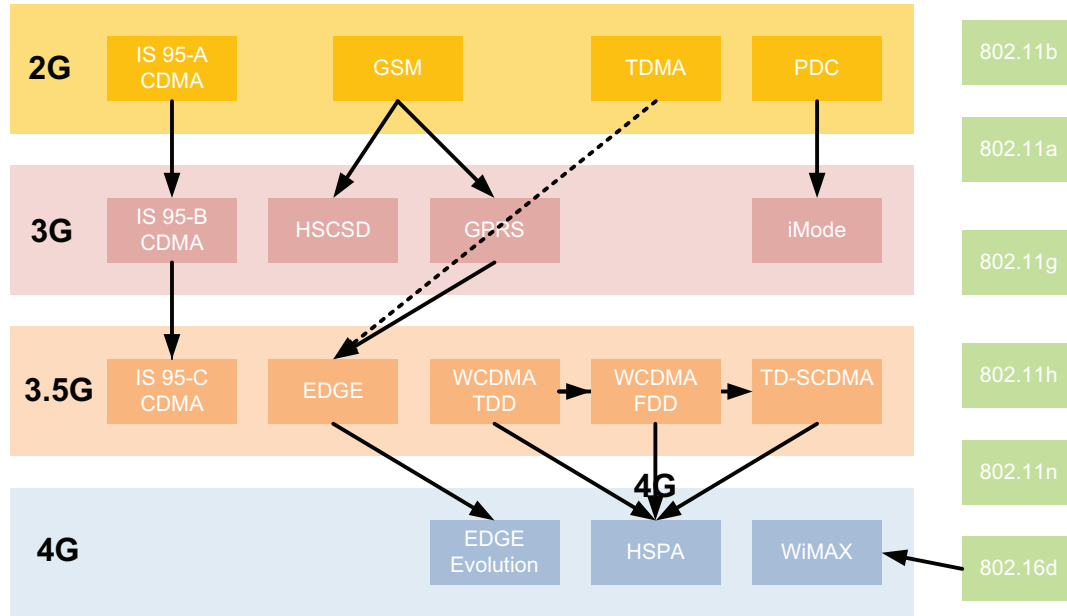


Figure 2.1: Evolution of wireless standards

In the widely-used wireless electronics industry, bandwidth, mobility, and range have constantly improved. A number of technologies have evolved with different bandwidths, carrier-frequencies, and modulation schemes, each one optimized to cater to a specific set of users. For long-range voice and data transfers, we have cellular standards like GSM, EDGE, and WCDMA. For home and office networks, and wireless personal networking, we have Wireless Local-Area Network (WLAN) standards like the 802.11a, 802.11b, and 802.11g (Figure 2.1). For short-range connectivity, we have Bluetooth and Ultra-Wide-Band.

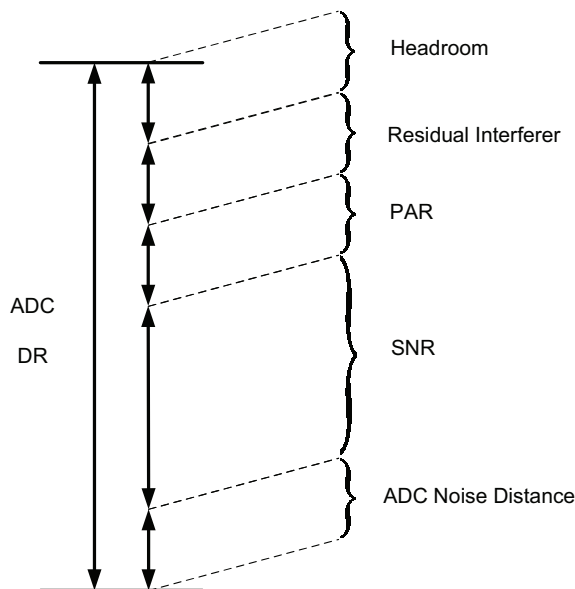


Figure 2.2: Required DR for ADC

To realize a power-optimal design, most of the processing - channel and band selection - should be done in the digital domain, mandating a conversion of the real-world analog signal to its discrete digital counterpart as early in the receiver chain as possible. The challenge now lies in faithfully encoding the analog signal in the presence of all the unwanted signals or interferers without overloading the Analog-to-Digital Converter (ADC) and without consuming a lot of power. Shown in Figure 2.2 is the system-level dynamic-range budgeting at its simplest. It depends strongly on the kind of coding employed by the standard and the interferers located close by in the spectrum.

Based on Figure 2.2, Table 2.1 shows the required dynamic-range specification on the ADC for different standards.

To enable users to be connected anywhere and at anytime, the industry has been on a constant lookout for the ultimate solution - an ultra-low-power intelligent radio, also called the cognitive radio. This is a single software-defined radio, which is smart enough to sense the frequency spectrum, pick the one with minimum traffic, and program itself to work optimally in that band. For the consumers, features like high-speed data services for multimedia applications, support for concurrent voice and data communication and global roaming are highly desirable. For a designer, this translates to portability and reconfigurability.

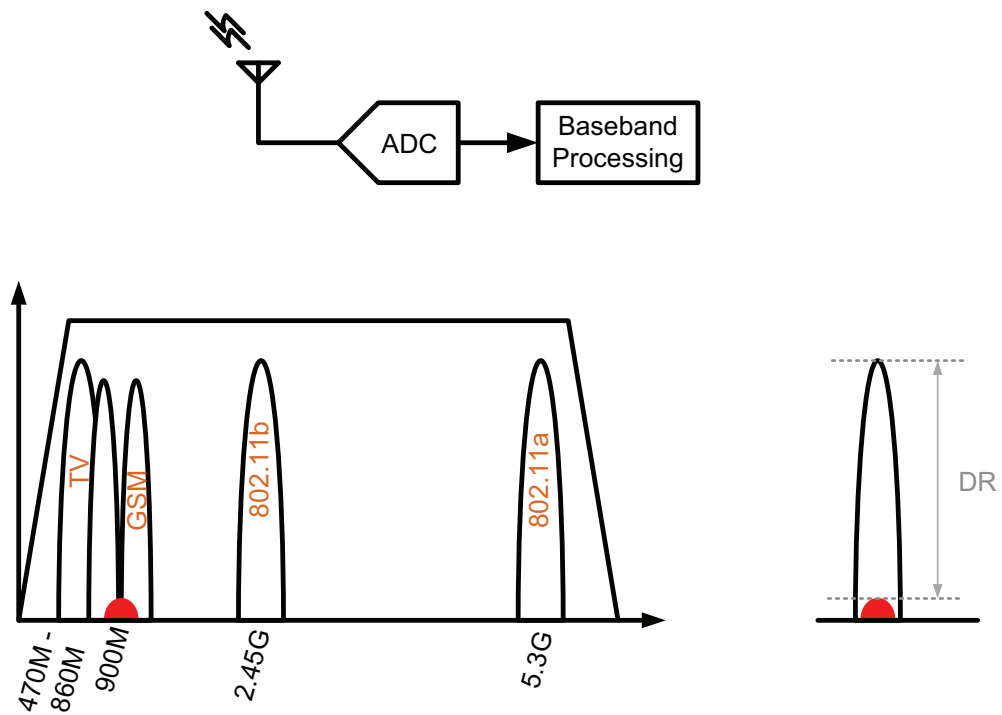


Figure 2.3: Software-Defined Radio

One proposed approach for this is the software-defined radio. As in Figure 2.3, the

preselect filter - which is usually discrete and off-chip - is eliminated. All the possible bands are received. The ADC is moved all the way up the chain and is capable of processing all the bands. But unfortunately, this mandates an 18-bit 10GS/s ADC - definitely not a power-optimal approach!!

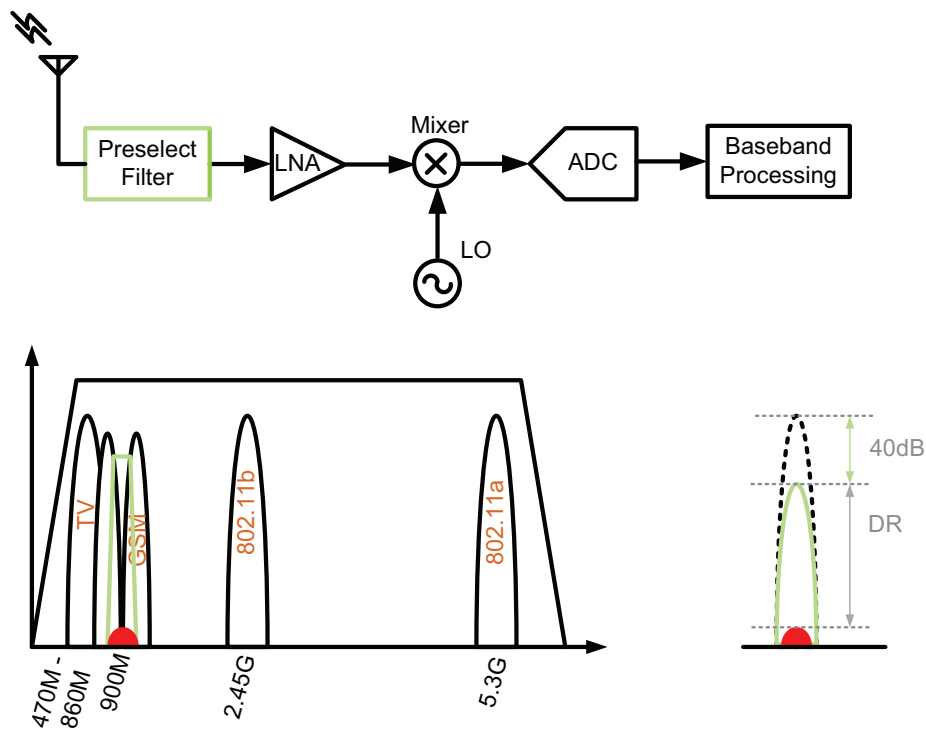


Figure 2.4: Traditional receiver with preselect filter

A more practical approach, is enabling channel-selection in receivers by using a preselect filter(Figure 2.4). The preselect filter attenuates the interferers, relaxing the requirements on the dynamic range(DR) of the ADC. Higher the filtering, lower is the required DR. But, this would mean that the preselect filter have a steeper roll-off or

higher-Q.

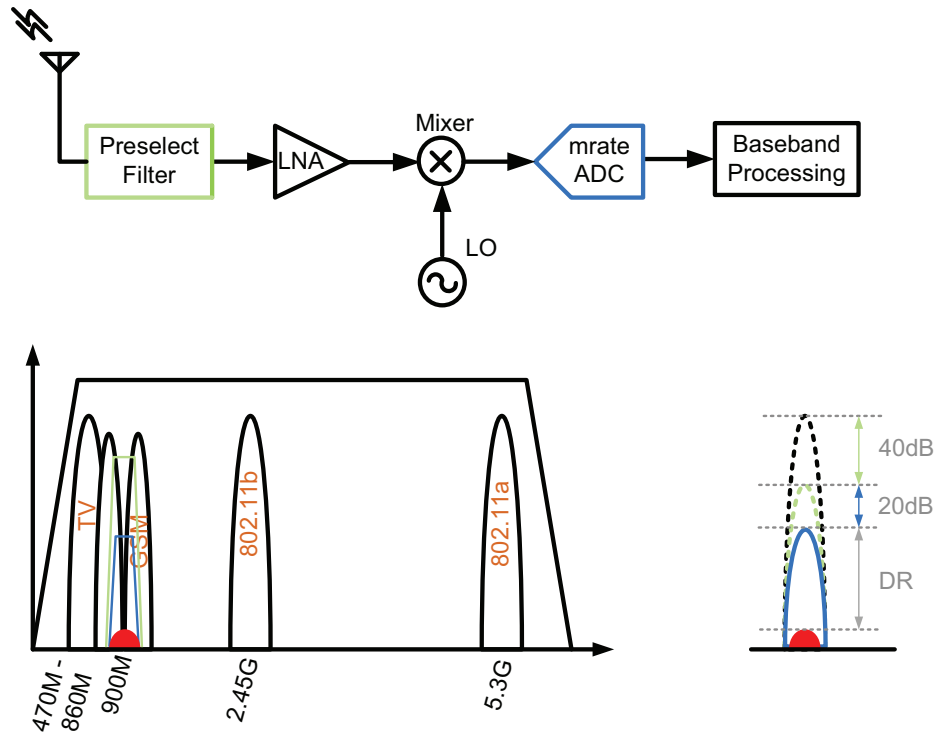


Figure 2.5: Traditional receiver with preselect filter and multi-rate ADC

However, if the ADC used is continuous time in nature or has in-built anti-aliasing, it will then provide one more level of filtering for signals beyond f_s , thereby reducing the DR requirements further(Figure 2.5) [15].

If the ADC is continuous-time in nature(Figure 2.6), there is no re-sampling of thermal noise nor clock feed-through. But, it suffers from sensitivity to clock-jitter and EMI. Reconfiguring it will require tuning of the passive-components. Since RC time-constants can vary upto 25% without tuning, the system clock could also vary by the

Table 2.1: ADC requirements

	GSM	WCDMA	UWB
Headroom(dB)	10	10	6
PAR (dB)	3	12	9
Residual Interferers(dB)	45	20	5
SNR(dB)	10	-8	6
ADC Distance(dB)	20	20	10
Required DR(dB)	88	54	36
ENOB	14	9	6
BW(Hz)	200K	200M	500M

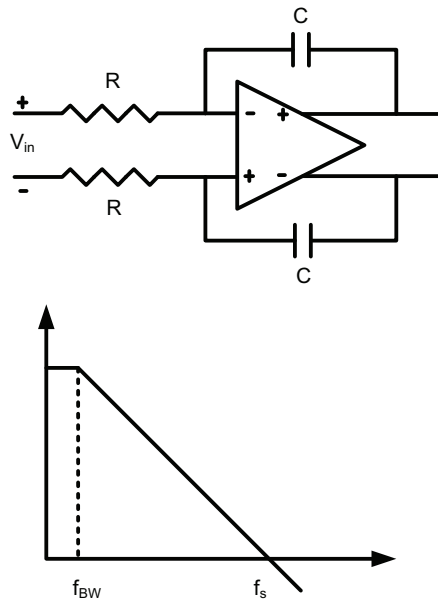


Figure 2.6: Continuous-time integrator

same amount.

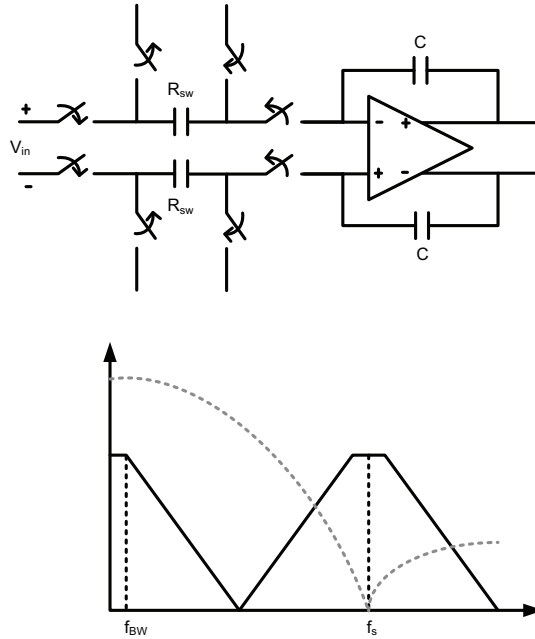


Figure 2.7: Discrete-time integrator

However, a discrete ADC, on the other hand (Figure 2.7), has a transfer function that scales with frequency. Also, its power consumption scales with the clock-frequency. The capacitors provide better matching and hence, the discrete ADC is more tolerant to jitter. To combine the best of both these, [16] proposes a two-stage $\Sigma - \Delta$ ADC where the first-stage is continuous but the second-stage is discrete. In other words, if we were to revisit Table 2.1, and assume an additional 6dB of filtering on the interferers due to the filtering properties of the ADC, the DR requirements will change table 2.2

But, the first-stage need not be continuous. Using a discrete-time front end, will

Table 2.2: Relaxed ADC requirements

	GSM	WCDMA	UWB
Headroom(dB)	10	10	6
PAR (dB)	3	12	9
Residual Interferers(dB)	45	20	5
Additional Attenuation(dB)	6	6	6
SNR(dB)	10	-8	6
ADC Distance(dB)	20	20	10
Required DR(dB)	82	48	30
ENOB	13	8	5
BW(Hz)	200K	200M	500M

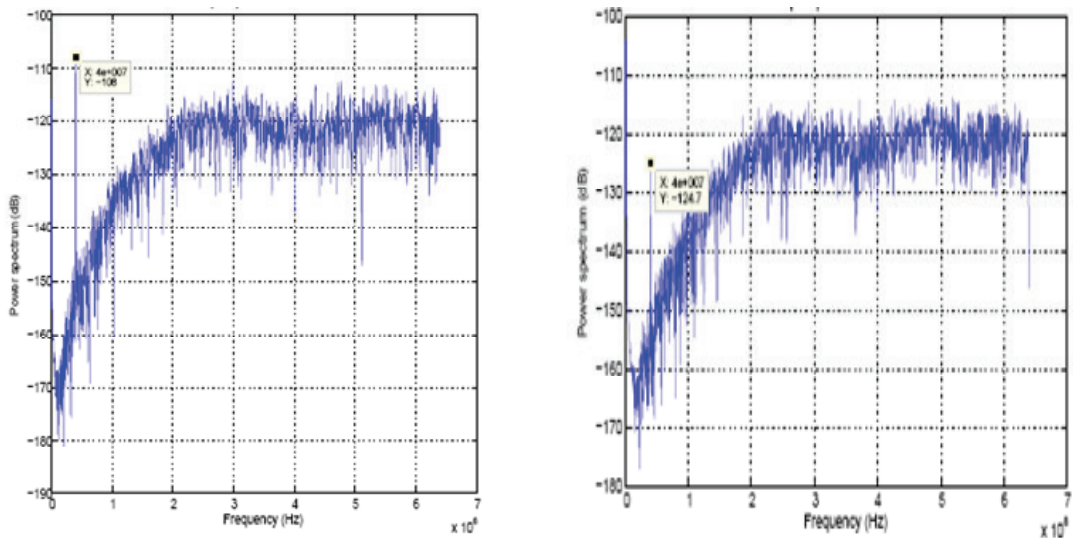


Figure 2.8: Reduced required DR for Multi-rate ADC

result in aliasing of $n \cdot f_s \pm \delta$ into the signal band. The preselect filter, attenuates interferers far away from its cut-off frequency. We only need to worry about the interferers that are closer to the cut-off frequency. If the strongest interferer is at $n \cdot f_s$, then the first stage needs to operate at $n \cdot f_s$. SIMULINK modeling and simulations are shown in Figure 2.8 for the worst-case where the interferer is at $2 \cdot f_s$. The PSD plots prove that just by operating the first stage at $2 \cdot f_s$, the proposed architecture provides interferer attenuation close to that of a continuous-time front-end. Beyond $2 \cdot f_s$ is the region of diminishing returns. This leads us to the architecture which has been referred to as the “multi-rate $\Sigma - \Delta$ ADC” in this dissertation.

2.2 Multi-Rate $\Sigma - \Delta$ Converter

2.2.1 Intuitive Approach to Multi-Rate $\Sigma - \Delta$ Converters

To further understand how the multi-rate $\Sigma - \Delta$ ADC works, let's consider the block-diagram of a traditional $\Sigma - \Delta$ ADC presented in Figure 2.9.

The loop-filter, $H(z)$ appears in the signal path for $X(z)$.

$$\begin{aligned}
 STF &= \left| \frac{Y(z)}{X(z)} \right| \\
 &= \left| \frac{A_c \cdot H(z)}{1 + A_c \cdot H(z)} \right| \approx 1
 \end{aligned} \tag{2.1}$$

However, for effect on quantization noise ($E_q(z)$), the loop-filter appears in the feed-back

path.

$$\begin{aligned}
 NTF &= \left| \frac{Y(z)}{E_q(z)} \right| \\
 &= \left| \frac{1}{1 + A_c \cdot H(z)} \right| \\
 &\approx \frac{1}{A_c \cdot H(z)} \tag{2.2}
 \end{aligned}$$

Hence, we see the inverse of the low-pass loop-filter function i.e. a high-pass response for the noise-transfer function, [17], [18].

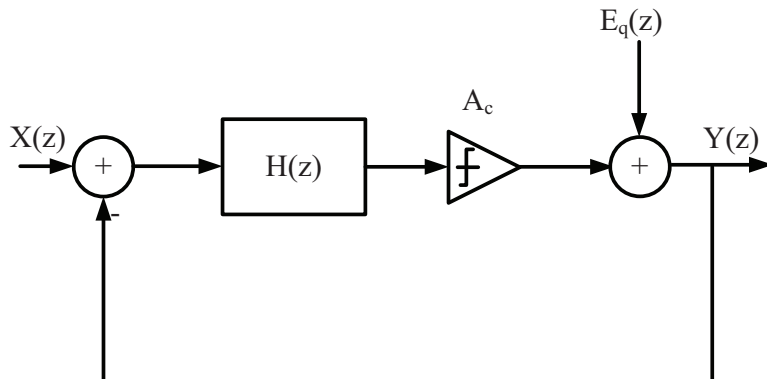


Figure 2.9: Block-diagram of a $\Sigma - \Delta$ ADC

In other words, at in-band frequencies, where the loop-filter has infinite-gain, the signal sees a unity-gain feedback but the quantization noise gets attenuated. The quantization noise thus gets shaped away from the band of interest.

Now, considering that the input is sampled at $f_{s,in}$ and that a down-sampling occurs at the loop-filter, $H_2(z)$ to a lower frequency - f_s .

The signal transfer function is still approximately unity.

$$\begin{aligned}
STF &= \left| \frac{Y(z)}{X(z)} \right| \\
&= \left| \frac{A_c \cdot H_1(z) \cdot H_2(z)}{1 + A_c \cdot H_1(z) \cdot H_2(z)} \right| \\
&\approx 1
\end{aligned} \tag{2.3}$$

The noise-transfer function is the inverse of the loop-filters.

$$\begin{aligned}
NTF &= \left| \frac{Y(z)}{E_q(z)} \right| \\
&= \left| \frac{1}{1 + A_c \cdot H_1(z) \cdot H_2(z)} \right| \\
&\approx \frac{1}{A_c \cdot H_1(z) \cdot H_2(z)}
\end{aligned} \tag{2.4}$$

And, the images $n \cdot f_{s,in} \pm \delta$ see a unity-gain response and appear at the output. But images resulting from the second stage of sampling to $f_s - n \cdot f_s \pm \delta$ - see an attenuation equivalent to the gain stages preceding the down-sampler i.e $H_1(z)$.

$$\begin{aligned}
ImageTF &= \left| \frac{Y(z)}{X_{im}(z)} \right| \\
&= \left| \frac{A_c \cdot H_2(z)}{1 + A_c \cdot H_1(z) \cdot H_2(z)} \right| \\
&\approx \frac{1}{H_1(z)}
\end{aligned} \tag{2.5}$$

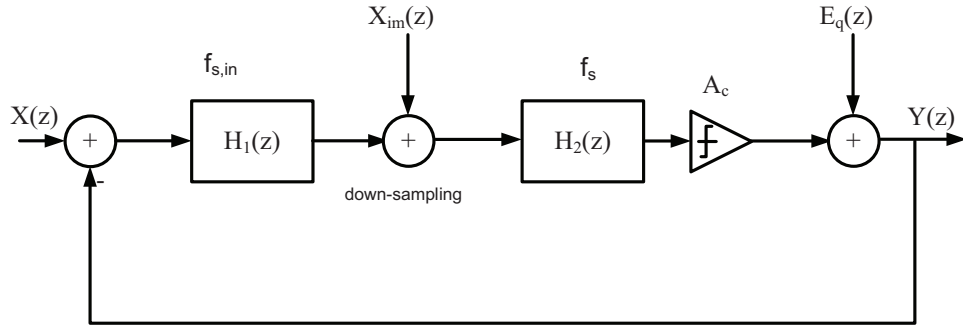


Figure 2.10: Block-diagram of a second-order $\Sigma - \Delta$ ADC

2.2.2 Review of Multi-Rate Signal Processing Concepts

To mathematically derive the equations that govern the multi-rate ADC, let's review the linear multi-rate discrete-time systems. Linear multi-rate systems have two more fundamental components in addition to the unit delay, the adder and the multiplier - the decimator and the interpolator [19], [20].

Decimator

The decimator of Figure 2.11(a) is characterized by the input-output relation given by

$$x_d[n] = x[Mn] \quad (2.6)$$

i.e. the output at time 'n' is equal to the input at time 'Mn'. Only the input samples that only occur at multiples of 'M' are retained as shown in Figure 2.11(b). In other words, the sampling rate is reduced by a factor of 'M'. Figure 2.11(c) shows the frequency domain plots of the output for an example input. The compression in time

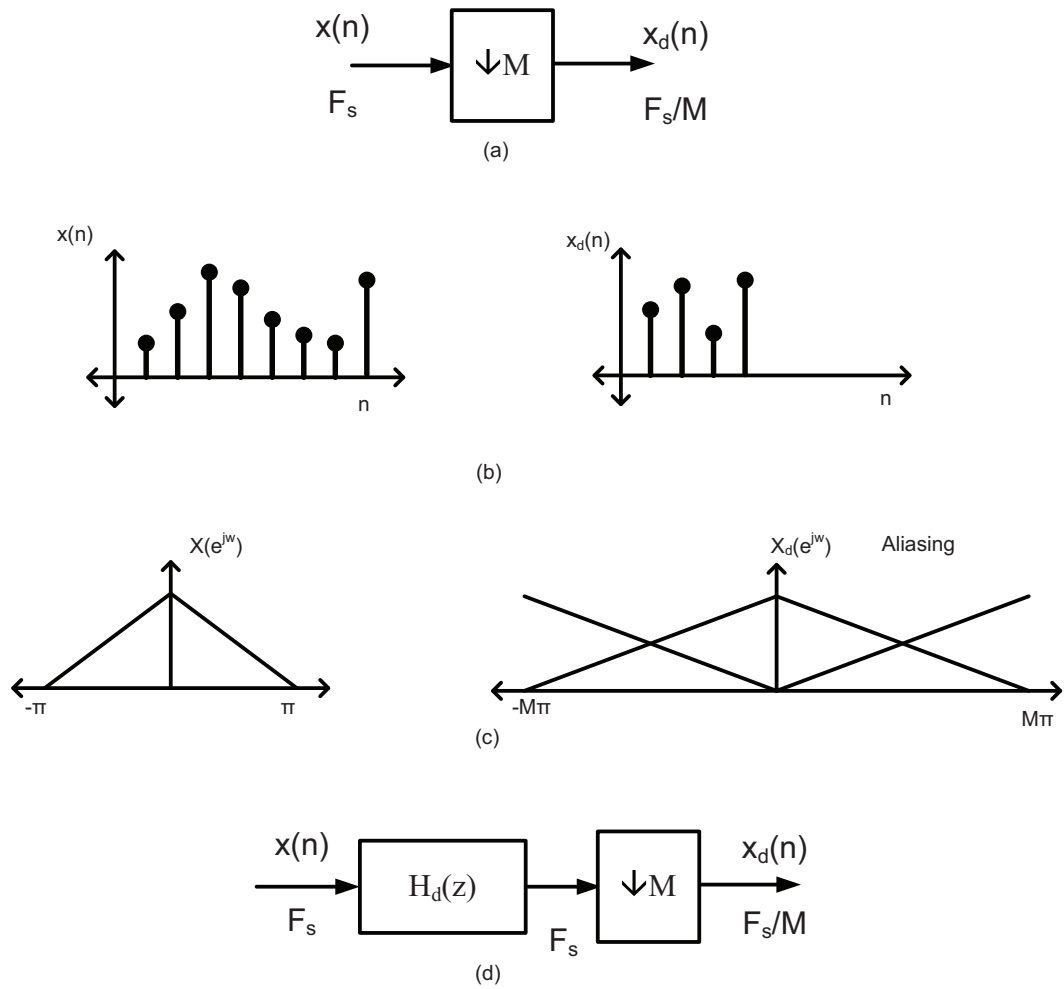


Figure 2.11: (a)Decimation (b)Time-Domain plot (c)Frequency-domain plot (d)Anti-aliasing filters

domain results in a stretching effect in the frequency-domain. The z-transform is given by

$$X_d(z) = \frac{1}{M} \sum_{k=0}^{M-1} X(z^{1/M} \cdot W^k) \quad (2.7)$$

The term with $k = 0$ is the stretched version of $X(z)$. While the other $(M - 1)$ terms are uniformly shifted versions of the stretched versions also known as the aliasing terms. As long as the $x[n]$ is bandlimited to π/M the aliases don't overlap and the signal can be recovered. Hence, most decimators are preceded by the decimating or anti-aliasing filters $H_d(z)$ of Figure 2.11(d). These filters are primarily, low-pass filters that bandlimit the input signal to avoid the ill-effects of aliasing.

Interpolator

The interpolator of Figure 2.12(a) is characterized by the input-output relation given by

$$x_i[n] = \begin{cases} x[\frac{n}{L}] & \text{if } n \text{ is a multiple of } L \\ 0 & \text{otherwise} \end{cases}$$

i.e. the output sequence is obtained by adding $(L - 1)$ samples of zero to the input sequence as shown in Figure 2.11(b) for $L = 2$. In other words, the sampling rate is increases by a factor of 'L'. Figure 2.11(c) shows the frequency domain plots of the output for an example input. The stretching in time domain results in a compression effect in the frequency-domain. The z-transform is given by

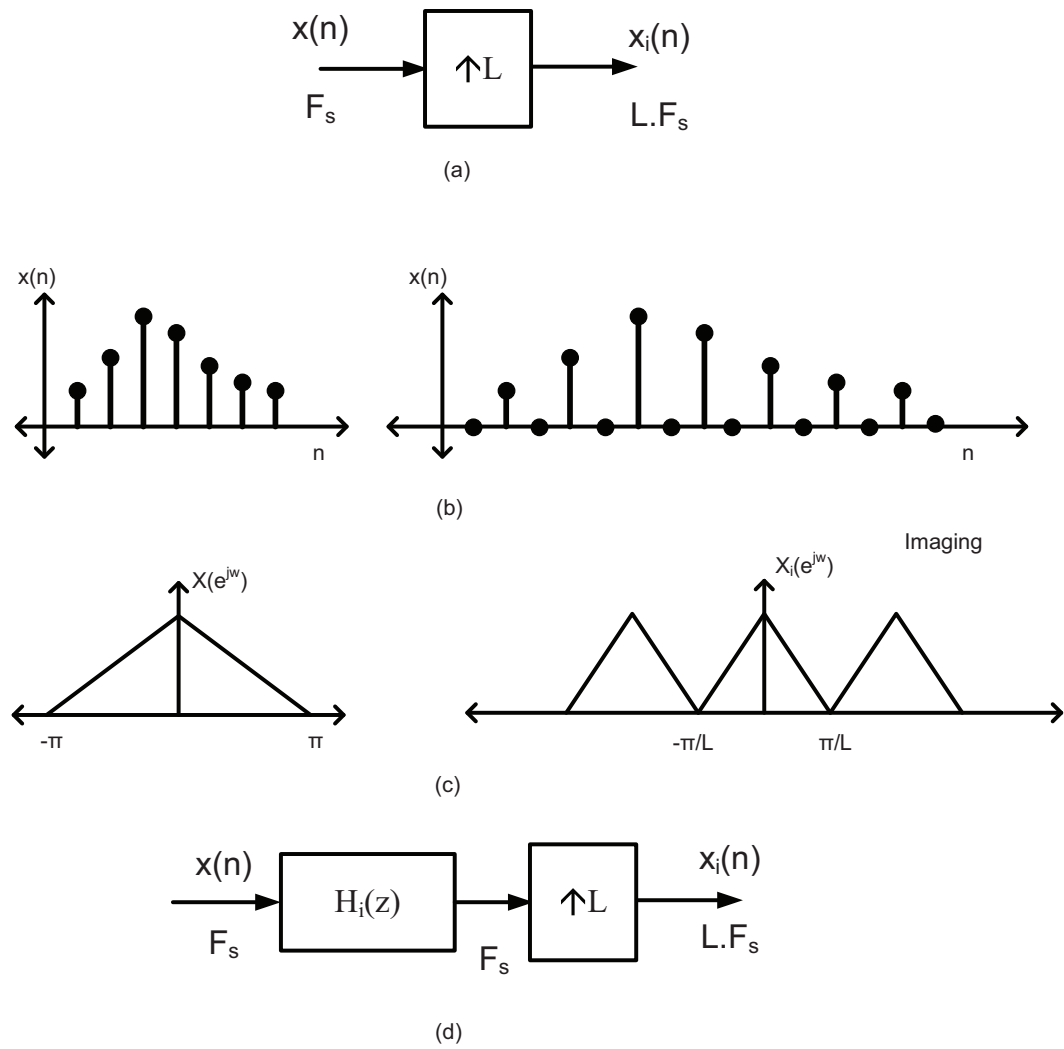
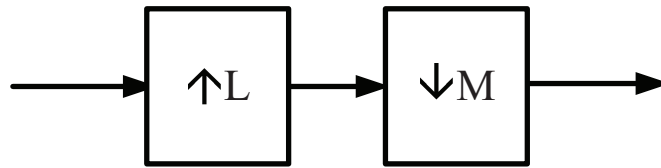


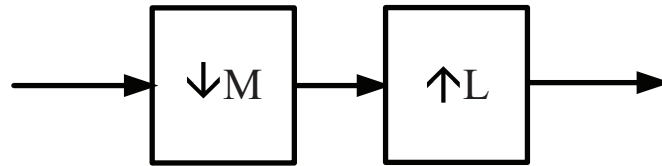
Figure 2.12: (a) Interpolation (b) Time-Domain plot (c) Frequency-domain plot (d) Interpolating filters

$$X_i(z) = X(z^L) \quad (2.8)$$

The interpolator output is thus an L-fold compressed version of the input. The appearance of the multiple copies of the input is known as the imaging effect. The fundamental difference between aliasing and imaging is that imaging does not lead to any loss of information as none of the time domain samples are lost. Most interpolators are followed by interpolating filters $H_i(z)$ of Figure 2.11(d). These filters are also low-pass filters which are used eliminate the images that result due to the up-sampling.



(a)



(b)

Figure 2.13: Cascade connections

Cascading Connections

Shown in Figure 2.13 are two possible cascading interconnections which are not interchangeable. The system shown in Figure 2.13(a) does not cause a loss of information

and is an identity system for $M = L$. But, the system of Figure 2.13(b) causes a loss of $M - 1$ of M samples.

Noble Identities

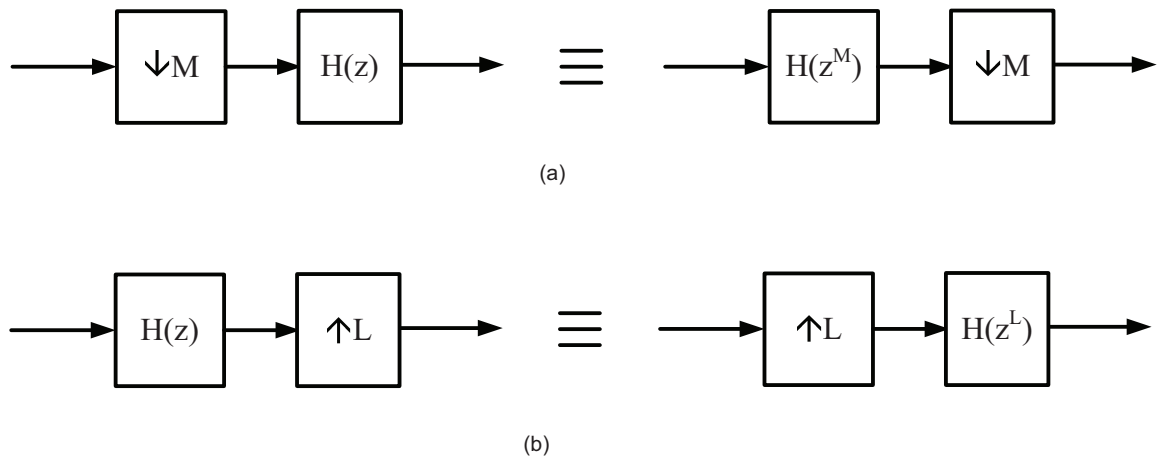


Figure 2.14: Noble Identities

In Figure 2.14(a) we have a decimator followed a filter $H(z)$. It can be proved based on Equation 2.7 that it is equivalent to $H(z^M)$ followed by the decimator, if the function $H(z)$ is rational. Likewise, from Equation 2.8, it follows that a filter $H(z)$ followed by an interpolator is equivalent to a filter $H(z^{1/L})$ followed by an interpolator, if the function $H(z)$ is rational, as shown in Figure 2.14(b). These are known as the “Noble Identities” and are used extensively in efficient implementations of filters and filter-banks [21].

Polyphase Transformation

A transfer function $H(z)$ can be decomposed into its polyphase components E_i as

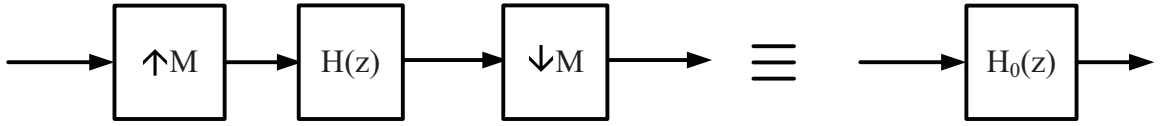


Figure 2.15: Polyphase Transformation

$$H(z) = \sum_{k=0}^{M-1} z^{-k} E_k(z^{-M}) \quad (2.9)$$

where M is the integral up-sampling ratio [21]. From the polyphase decomposition, it can be shown that the cascade of an up-sampler, a filter $H(z)$ and a down-sampler is equivalent to the 0^{th} polyphase component of $H(z)$ as in Figure 2.15.

2.2.3 Analytical Approach to Multi-Rate $\Sigma - \Delta$ Converters

To find the NTF of the proposed multi-rate $\Sigma - \Delta$ system, one can reduce the multi-rate $\Sigma - \Delta$ Converter of Figure 2.16 to a system as shown in Figure 2.17, by applying the superposition theorem.

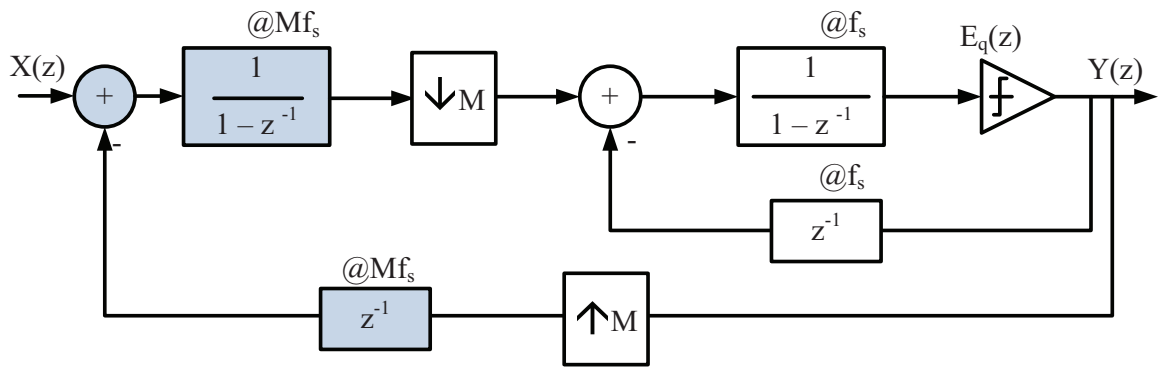


Figure 2.16: Block-diagram of the Multi-rate $\Sigma - \Delta$ Converter

Using the noble identities of Figure 2.14, the first stage of the converter that runs

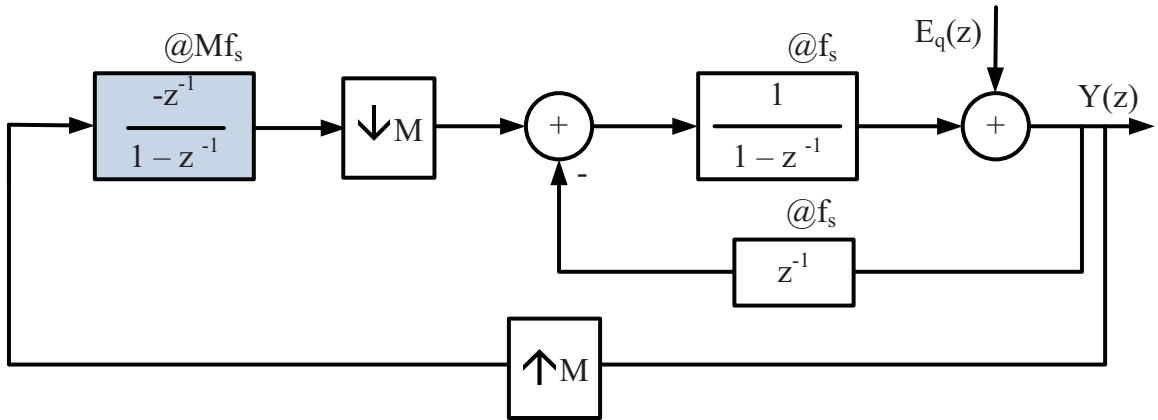


Figure 2.17: Applying superposition theorem to the Multi-rate $\Sigma - \Delta$ Converter

at Mf_s can be transformed to running at f_s . Note that the system of Figure 2.18 is now a single-rate system at f_s .

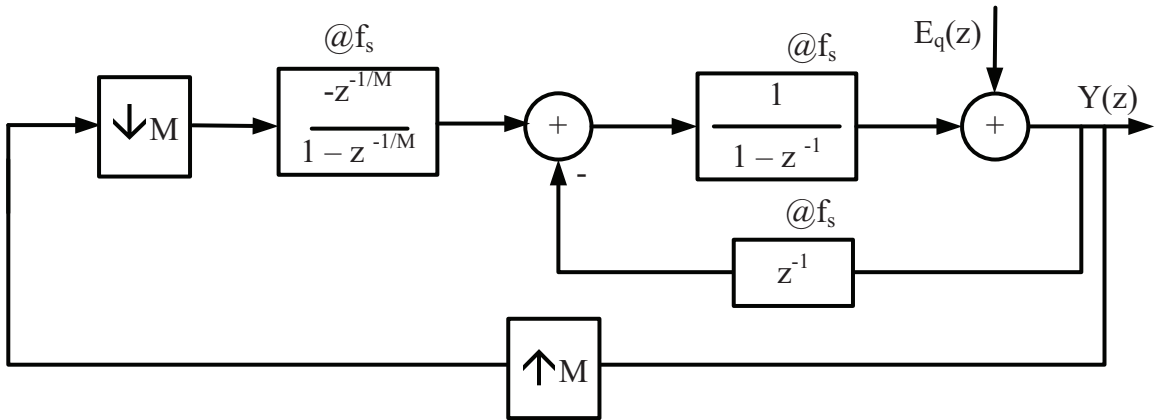


Figure 2.18: Applying “Noble Identities” to the Multi-rate $\Sigma - \Delta$ Converter

The cascaded up-sampler followed by down-sampler is a identity system described in Figure 2.13(a).

The NTF of the system can finally be reduced to

$$NTF = \left| \frac{Y(z)}{E_q(z)} \right|$$

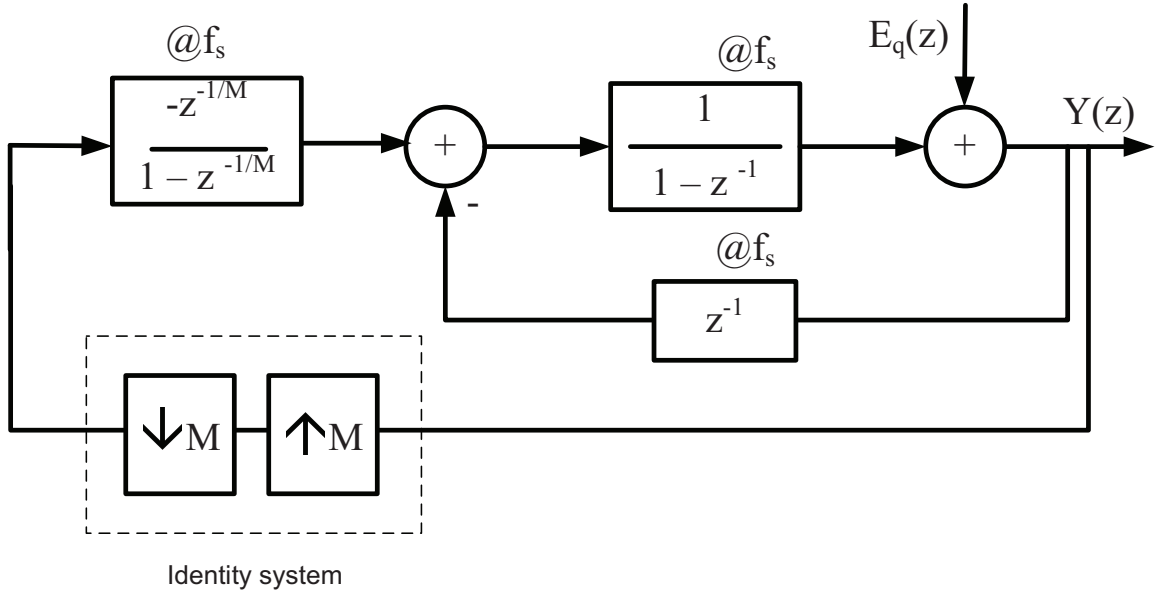


Figure 2.19: Single-rate equivalent of the Multi-rate $\Sigma - \Delta$ Converter

$$= |(1 - z^{-M}) \cdot (1 - z^{-1})| \quad (2.10)$$

2.3 Multi-Rate $\Sigma - \Delta$ Converter Architectures

Figure 2.20 shows a model of the traditional second-order $\Sigma - \Delta$ ADC. Both the stages operate at a sampling frequency of $OSR \cdot f_{in}$ where OSR is the “*Over-Sampling Ratio*”.

If $X(z)$ is the input and $E_q(z)$ is the quantization noise of the comparator, then the output of the ADC, $Y(z)$ is given by Equation 2.11 [22].

$$Y(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^2 \cdot E_q(z) \quad (2.11)$$

The noise-transfer function is given by Equation 2.12.

$$\begin{aligned}
 NTF &= \left| \frac{Y(z)}{E_q(z)} \right| \\
 &= |(1 - z^{-1})^2| \\
 &\approx \frac{4\pi^2 f^2}{f_s^2}
 \end{aligned} \tag{2.12}$$

And, the SNR is calculated to be [22] -

$$SNR_{max} = 6.02 \cdot N + 30 \log(OSR) - 3.4 \tag{2.13}$$

where, N is the number of levels in the quantizer and OSR is the over-sampling ratio.

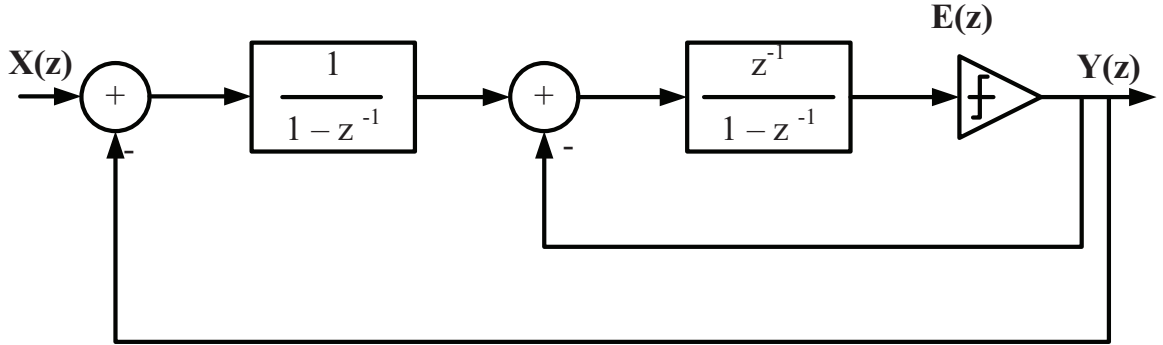


Figure 2.20: Block-diagram of traditional $\Sigma - \Delta$ ADC

2.3.1 Multi-rate $\Sigma - \Delta$ Converter

Figure 2.21 shows the proposed multi-rate $\Sigma - \Delta$. As depicted, the only difference from the traditional second-order $\Sigma - \Delta$ ADC is that the first stage runs at $2 \cdot f_s$. The second stage of both the architectures run at f_s . The feedback is at f_s but gets up-sampled to $2 \cdot f_s$.

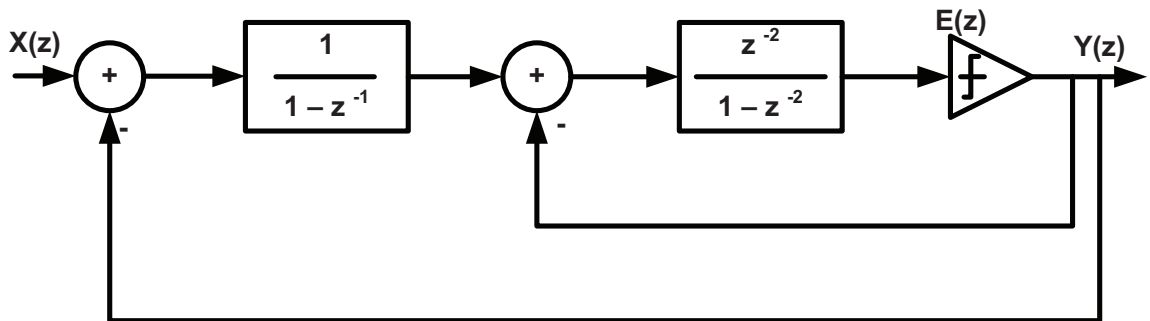
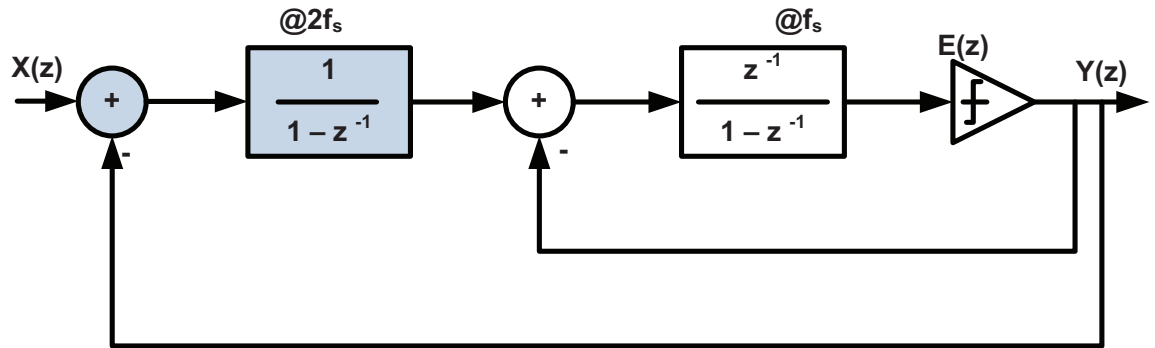


Figure 2.21: Block-diagram of multi-rate $\Sigma - \Delta$ ADC

The proposed architecture can be modeled by applying the simple transformation of $z^{-1} \rightarrow z^{-2}$ to the second-stage. Also, replacing the comparator by a unity-gain block and applying the superposition theorem to calculate the noise transfer function(NTF), we find that noise-transfer function(NTF) is given by

$$\begin{aligned}
NTF &= \left| \frac{Y(z)}{E_q(z)} \right| \\
&= \left| \frac{1}{1 - \left(1 + \frac{1}{1 - z^{-1}}\right) \left(\frac{z^{-2}}{1 - z^{-2}}\right)} \right| \\
&= \left| \frac{1}{1 + \frac{z^{-2} \cdot (2 - z^{-1})}{(1 - z^{-1}) \cdot (1 - z^{-2})}} \right| \\
&= \left| \frac{z^{-3} - z^{-2} - z^{-1} + 1}{2z^{-3} - 3z^{-2} - z^{-1} + 1} \right| \tag{2.14}
\end{aligned}$$

The NTF of Equation 2.14 shows a high-pass response with the gain at DC and very low frequencies being zero. As expected, the quantization-noise gets shaped away from DC frequencies.

The signal transfer function(STF), can also be calculated in a similar way -

$$\begin{aligned}
STF &= \left| \frac{Y(z)}{X(z)} \right| \\
&= \left| \frac{z^{-1}}{1 + z^{-1} - z^{-1/2}} \right| \tag{2.15}
\end{aligned}$$

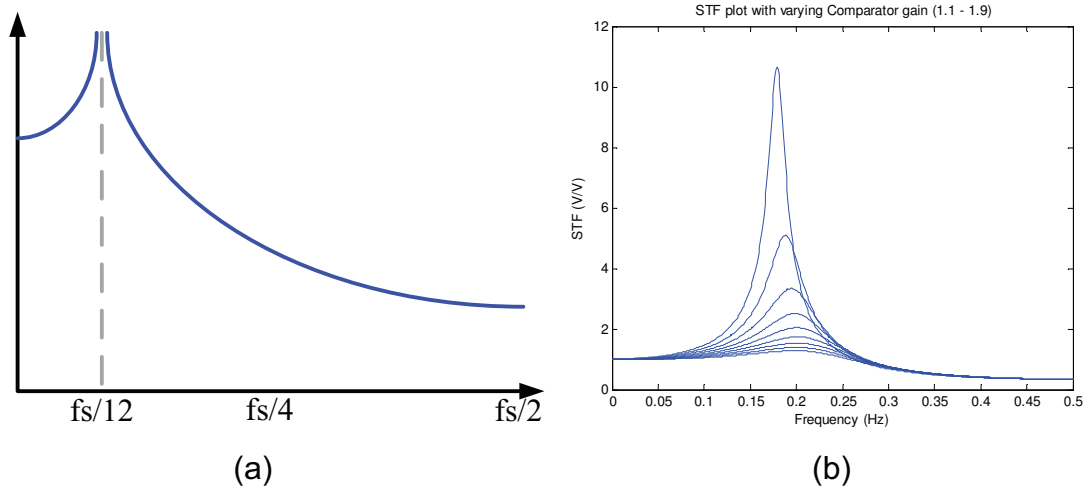


Figure 2.22: STF plot of multi-rate $\Sigma - \Delta$ ADC

The STF shows a band-pass response with the gain at DC and very low frequencies being unity and tapering off to $\frac{1}{3}$ at $f_s/2$. However, it exhibits resonance at $f_s/12$ as shown in Figure 2.22(a). It is to be noted that this occurs only when the comparator gain is unity. Figure 2.22(b) shows the STF plot versus A_c , the comparator gain. For all comparator gains greater than unity, there is only a peaking in the response and no resonance. If the comparator gain can be limited to always being greater than 1, or, in other words - if comparator overload is avoided, this resonance will not be an issue.

Figure 2.23 shows the power spectral density (PSD) of the output of the aforementioned multi-rate ADC in SIMULINK. The first stage runs at $2 \cdot f_s$ and the second stage runs at f_s and rate-transition blocks are inserted appropriately.

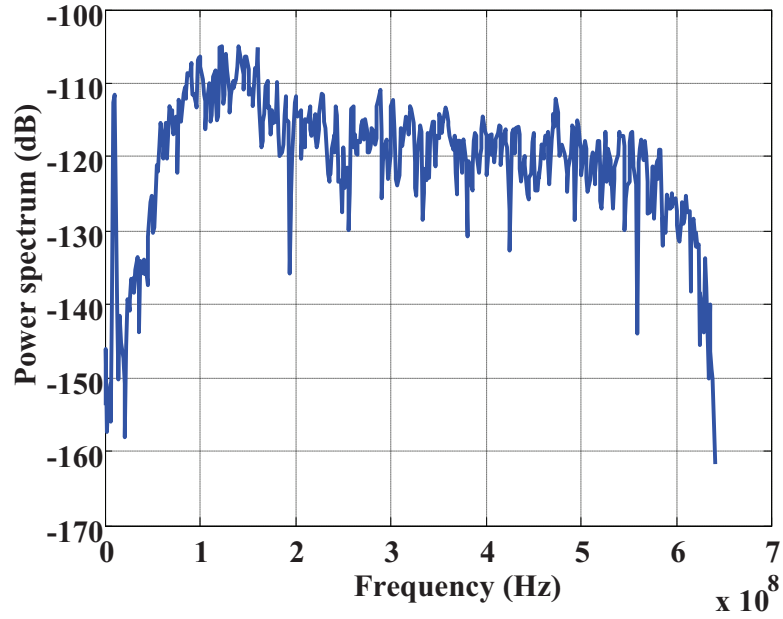


Figure 2.23: Output PSD plot from SIMULINK

2.3.2 Modified Multi-Rate $\Sigma - \Delta$ Converter

This section proposes a slight modification in the architecture to overcome the resonance in the STF for a comparator gain of unity. Figure 2.24(a) shows the block-diagram of the modified multi-rate $\Sigma - \Delta$ Converter. A delay element occurs in the feedback path of the converter and not in the forward-path. The first-stage and the feedback to it runs at $2 \cdot f_s$. The second-stage and the feedback to it runs at f_s .

Applying the $z^{-1} \rightarrow z^{-2}$ to the second-stage and inner-most feedback loop, the Block-diagram can be reduced to Figure 2.24(b) for further analysis. Writing out the transfer function of the system,

$$Y(z) = \frac{\frac{X(z) - z^{-1}Y(z)}{1 - z^{-1}} + z^{-2}Y(z)}{1 - z^{-2}} \quad (2.16)$$

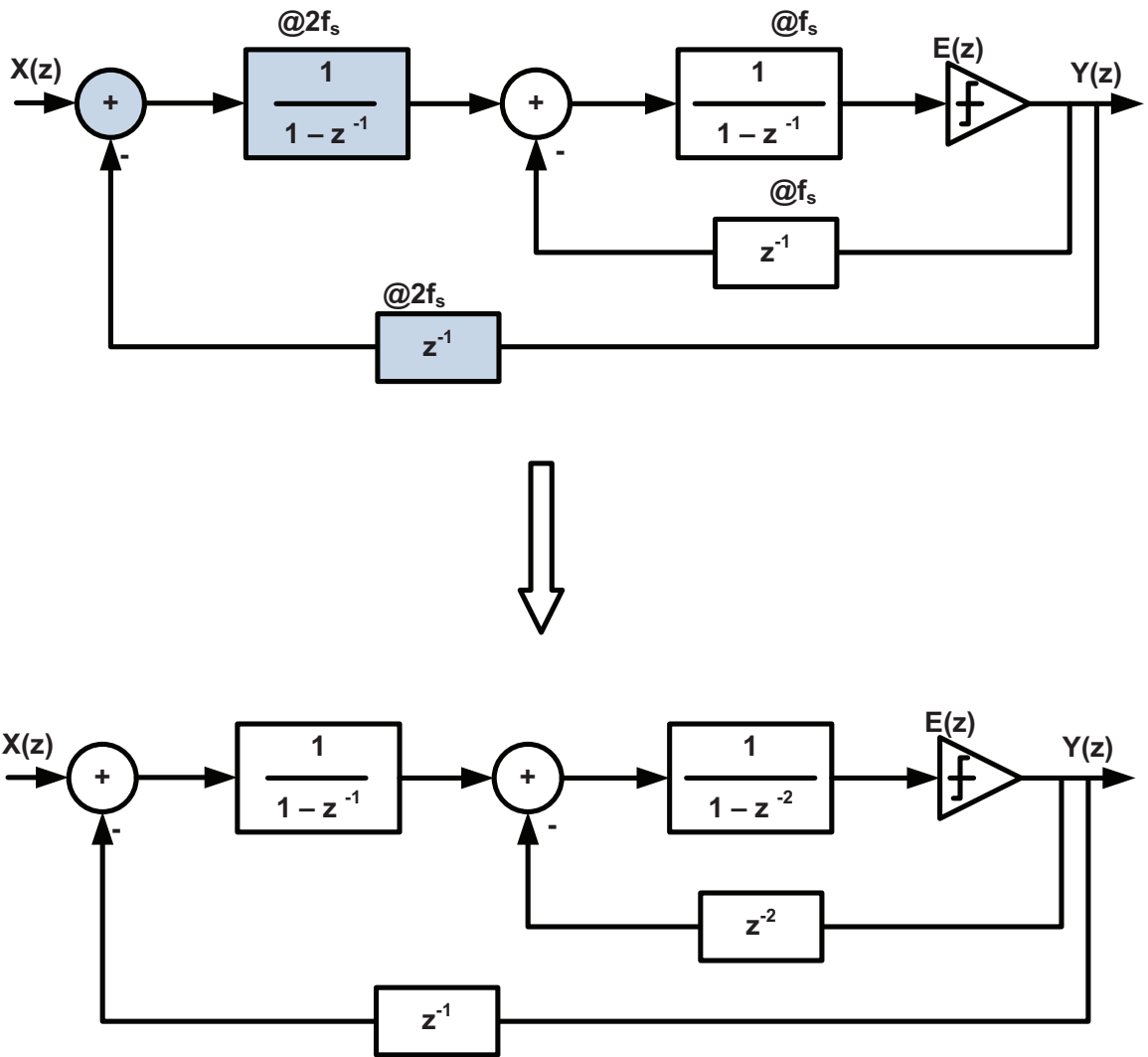


Figure 2.24: Block-diagram of the modified Multi-rate $\Sigma - \Delta$ ADC

$$Y(z) = X(z) + E_q(z) \cdot (1 - z^{-1}) \cdot (1 - z^{-2}) \quad (2.17)$$

where $X(z)$ represents the input and $E_q(z)$ represents the quantization noise.

Equation 2.17 shows that the system has a unity gain signal-transfer function.

$$STF = \left| \frac{Y(z)}{X(z)} \right| = 1 \quad (2.18)$$

The noise-transfer function is given by

$$NTF = |(1 - z^{-1}) \cdot (1 - z^{-2})| \quad (2.19)$$

$$NTF = 4 \sin \omega \cdot \sin\left(\frac{\omega}{2}\right) \quad (2.20)$$

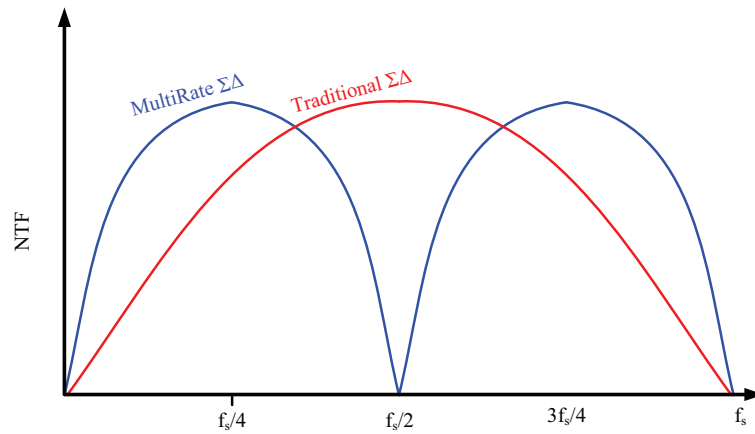


Figure 2.25: Noise Transfer Function of the Multi-rate $\Sigma - \Delta$ ADC

The NTF plot as shown in Figure 2.25 reveals NTF zeros at DC, $f_s/2$ and f_s . Higher frequencies will also have the sinc-shaping that comes with sampled data systems. It is this notch at $f_s/2$ that will considerably attenuate the images that will fall into

bandwidth of concern. This anti-aliasing, though not as complete as a CT-FE ADC, will alleviate the burden on the anti-aliasing filter preceding the ADC. The NTF has zeros at both DC and $f_s/2$. The maximum value of 1.732 occurs at $f_s/6$. The above approximation holds for sampling frequencies much greater than the bandwidth. The maximum value that δ can assume is 2. The SNR is calculated to be

$$\begin{aligned}
P_n &= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} |N(f)|^2 \sigma_n^2 df \\
&= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4 \sin^2 \left(\frac{2\pi f}{f_s} \right) \sin^2 \left(\frac{\pi f}{f_s} \right) \sigma_n^2 df \\
&\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} \left(\frac{2\pi f}{f_s} \right)^4 \sigma_n^2 df \\
&= \frac{2\pi^4 \sigma_n^2}{5 \cdot OSR^5} \tag{2.21}
\end{aligned}$$

If the ADC in the $\Sigma - \Delta$ converter has a resolution of N_{ADC} . The maximum SNR of this system is given by Equation(3.8).

$$SNR_{max} = 6.02N_{ADC} - 5.14 + 50 \log(OSR) \tag{2.22}$$

Figure 2.26 shows SIMULINK plot of the output power spectral density, confirming the NTF shape and providing proof of concept.

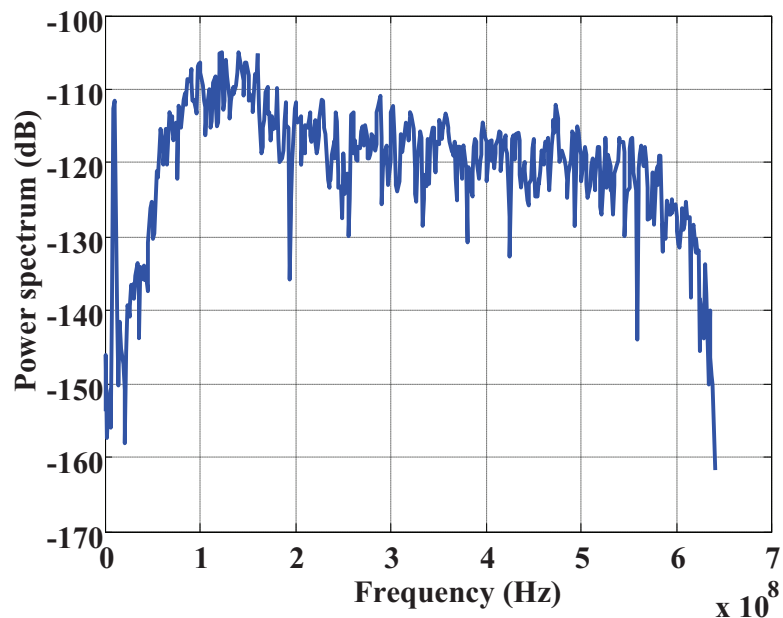


Figure 2.26: Output PSD plot from SIMULINK

2.4 Circuit Design and Implementation

The circuit of the multi-rate $\Sigma - \Delta$ ADC implemented in the test-chips is similar to that of a traditional second-order $\Sigma - \Delta$ ADC. The loop-filters are implemented as switched-capacitor filters. To prove the concept, the design was not optimized for power - no capacitor or bias scaling in the second stage. The comparator in the loop is a standard back to back latch with regenerative feedback.

Loop Filter

For the loop filters, switched-capacitor implementations of low-pass filters are employed. Shown in Figure 2.27 is the schematic of the loop filter. The input common mode is set to a voltage level - CMI. The output common-mode of each stage is set by a separate

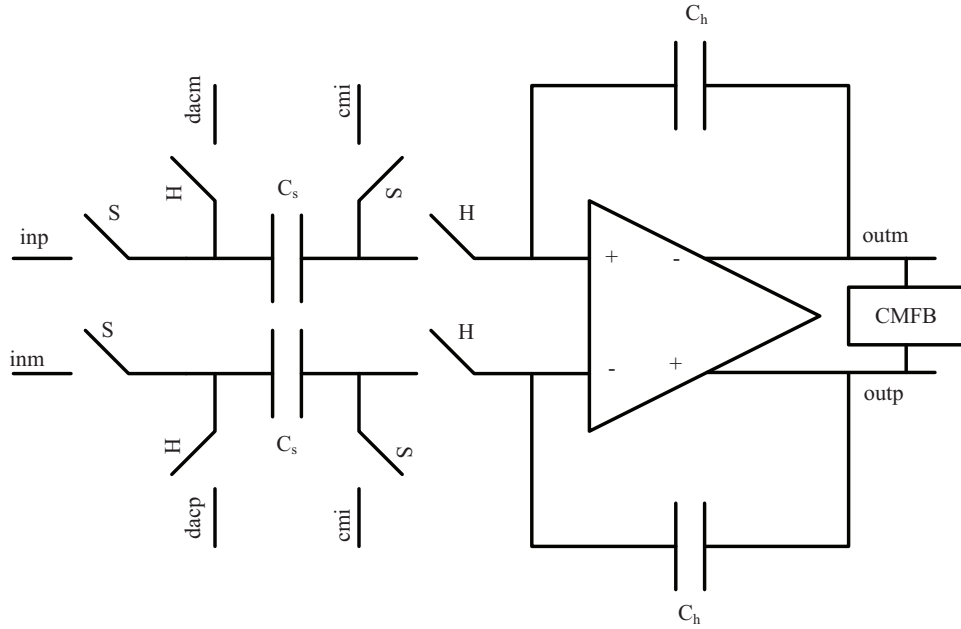


Figure 2.27: Switched-capacitor implementation of the loop filter

switched-capacitor common-mode feedback circuit. The input is sampled on to the C_s capacitors in the sampling phase and transferred on to the C_h capacitors in the hold-phase. In this architecture, the C_h capacitors are not reset but hold on to the output through the next sample phase. Based on the conservation of charge, the transfer function of the switched capacitor circuit can be written out to be as given in Equation 2.24.

$$C_s \cdot x[n] + C_h \cdot y[n - 1] = C_h \cdot y[n] \quad (2.23)$$

where $y(n) = outp(n) - outm(n)$ and $x(n) = inp(n) - inm(n)$.

$$\frac{Y(z)}{X(z)} = \frac{C_h}{C_s} \cdot \frac{1}{1 - z^{-1}} \quad (2.24)$$

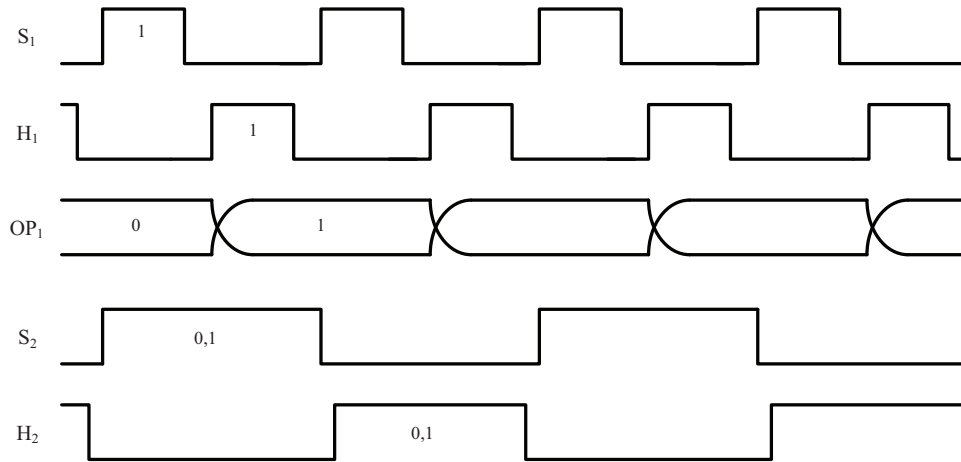


Figure 2.28: Clocking diagram of the loop filters

The clocking frequency of the first stage is twice the clocking frequency of the second stage. The sample and hold phases are derived as non-overlapping clock-phases of the master input clock as shown in the clocking diagram of Figure 2.28.

Comparator

The quantizer used is a simple clocked comparator with back-to-back latches and pre-amplifier biased at $20\mu A$. In the sample-mode, the outputs of the comparator are shorted and a differential current proportional to the differential input is fed to it. Thus, the comparator is in sample-mode, tracking the output of the filter all through the filter's hold-phase. Before the filter quits its hold phase, the comparator switches into its regeneration phase. Given the strong positive feedback loop, the output rails to one of the supplies. Shown in Figure 2.29 is the schematic diagram of the clocked comparator.

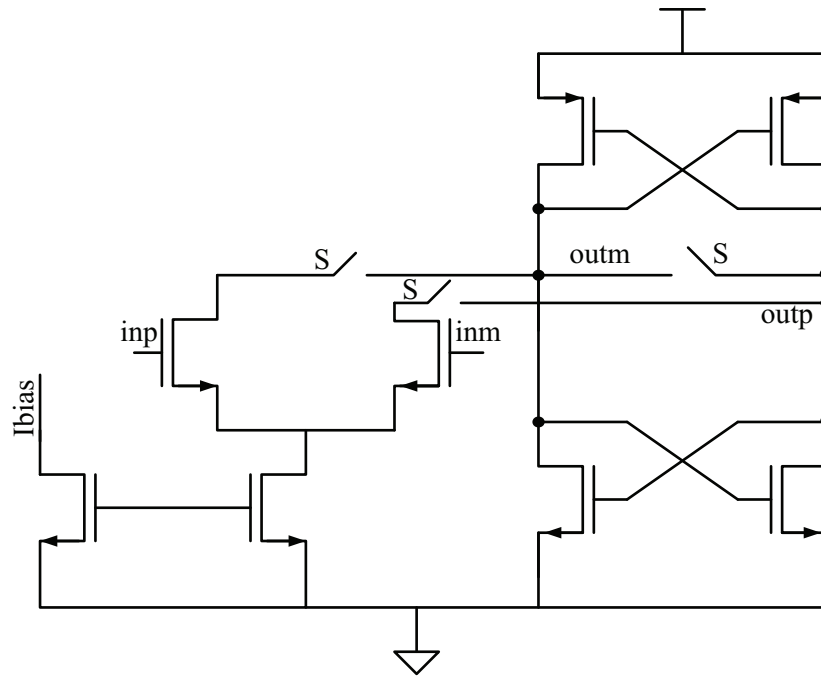


Figure 2.29: Schematic of the clocked comparator

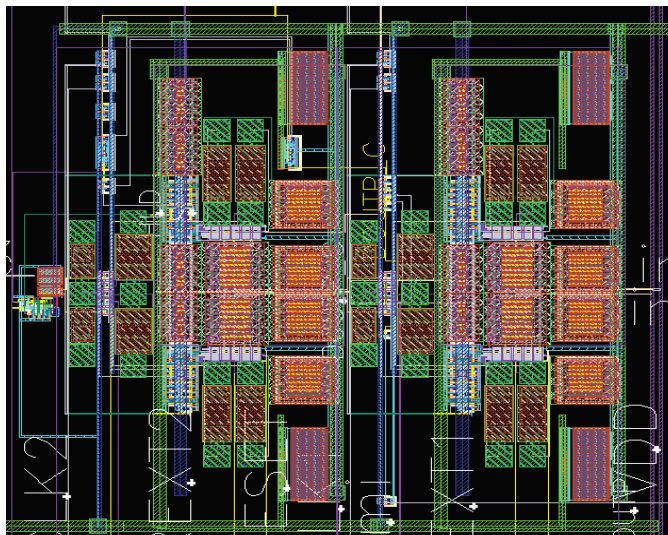


Figure 2.30: Layout of the Multi-Rate ADC in 0.13μ CMOS

2.5 Simulation Results

The design was implemented in 0.13μ CMOS process (Figure 4.7). Spectre simulations show about 25dB image suppression when the image is at 5MHz while the signal bandwidth is about 1MHz.

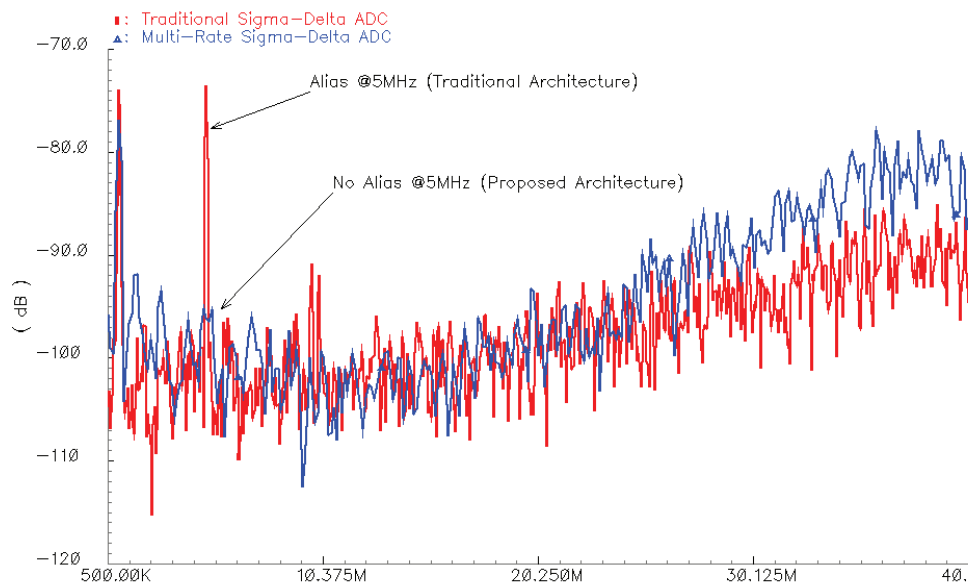


Figure 2.31: Spectre Simulation Results

Typically, the ADC consumes about $1.5mA$ from a $1.2V$ supply with the first stage running at $500MHz$.

2.6 Measurement Setup

Mounted on a PCB, the chip required a single-ended clock and differential inputs. Also, provided by the PCB are the 1V supplies, $REFP = 0.75V$, $REFN = 0.25V$, and a current bias provided by an external resistor(R_{EXT}). The clock signals are no more than $500MHz$ (and optional $1G$ for UWB), and hence the chip package is not the limiting factor. An Agilent E2244B will drive the required clock.

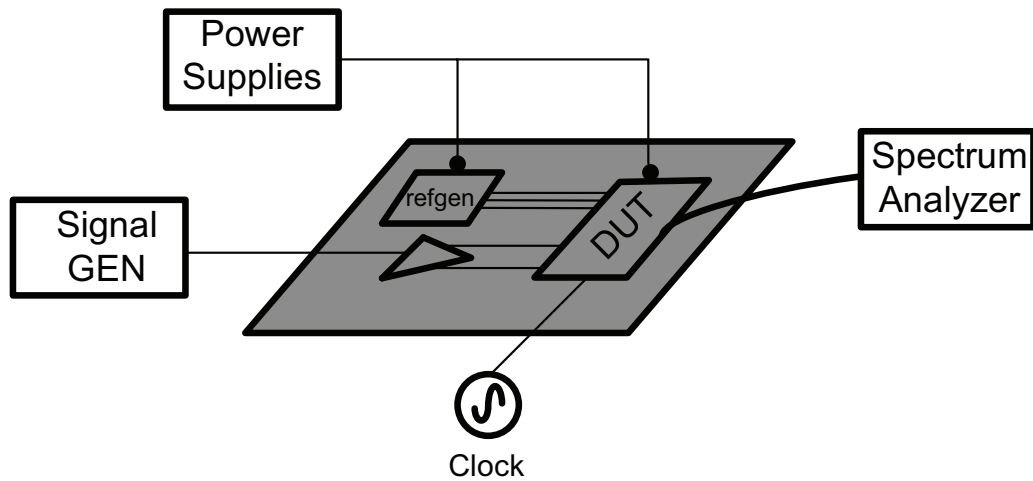


Figure 2.32: Test Setup for the multi-rate ADC

The inputs need to be differential with a common-mode of about $0.6V$ (CMI) upto about $500MHz$. A low-voltage differential amplifier is used for the single-ended to differential conversion of the single-ended input to feed into the chip. To calculate the SNR, the output is sampled and stored on a LeCroy 9350AL. With $500MHz$ BW and $1MB$ RAM, we get sufficient samples. This data is then ported into MATLAB to

calculate SNR. We use the same method to measure the power of the aliased signal and view the spectrum with an Agilent Spectrum Analyzer 8560(30 Hz to 2.9 GHz).

2.7 Conclusions

A novel multi-rate $\Sigma - \Delta$ ADC that makes the best use of the existing digital processes has been presented. While this paper deals with only a second-order $\Sigma - \Delta$, the concept can be extended to higher-order $\Sigma - \Delta$ ADCs. Further, in a multi-stage implementation, N can be greater than two with gradual down-sampling to the required f_s in the last-stage.

Table 2.3: Comparison of Traditional and Multi-Rate ADC

Type	—NTF—	SNR	ENOB
II Order - $\frac{f_s}{2}$	$\frac{4 \cdot \pi^2 \cdot f^2}{f_s^2} \cdot 4$	$\frac{60 \cdot 2^{2N} \cdot OSR^5}{32 \cdot 8 \cdot \pi^4} \approx X - 15\text{dB}$	$N - 2.5$ bits
II Order - f_s	$\frac{4 \cdot \pi^2 \cdot f^2}{f_s^2}$	$\frac{60 \cdot 2^{2N} \cdot OSR^5}{8 \cdot \pi^4} \approx X\text{dB}$	N bits
II Order - $f_s - \frac{f_s}{2}$	$\frac{4 \cdot \pi^2 \cdot f^2}{f_s^2} \cdot \delta$	$\frac{60 \cdot 2^{2N} \cdot OSR^5}{\delta^2 \cdot 8 \cdot \pi^4} \approx X - 6\text{dB}$	$N - 1$ bits

Chapter 3

Multi-Tone $\Sigma\Delta$ ADC

The zeros of the noise transfer function (NTF) of a $\Sigma\Delta$ converter can be altered by modifying the loop filter. For example, a low-pass $\Sigma\Delta$ is converted into a band-pass $\Sigma\Delta$ by shifting the zeros of the NTF from zero to $f_s/4$. In a similar fashion, an N-Tone $\Sigma\Delta$ can be created by inserting multiple zeros in the NTF. If the signals are then placed only in these noise valleys, a high Signal-to-Noise Ratio (SNR) can be achieved. In its most simplest form - the number of noise valleys being one - the N-Tone $\Sigma\Delta$ converter reduces to the familiar band-pass $\Sigma\Delta$ converter. Realized by a feedback loop around a resonator, the performance of the converter depends on the resonator characteristics. In other words, non-idealities in the resonator manifest themselves as a deterioration in the SNR. In this chapter, we look into the system-level analysis of an N-Tone $\Sigma\Delta$ converter, various possible modulator architectures and their performance. We also look into the various sources of non-idealities in the N-tone $\Sigma\Delta$ converter and their effect on the converter's SNR. We then present one low-power and another mismatch-insensitive implementation of such a converter.

3.1 Motivation

One of the alternatives for the high-rate ultra-wideband (UWB) standard (802.15.3a) [23] for short range multi-media communications is orthogonal frequency division multiplexing based (UWB-OFDM). This alternate implementation uses a signal bandwidth of 528MHz, offers high spectral efficiency and multi-path resolution[24]. However, the 528MHz signal bandwidth implies that the sample rate needs to be greater than 528MHz to avoid aliasing. Note that a 528MHz sample rate is sufficient as the signal does not contain quadrature information (as is normally the practice when spectrum is expensive) due to wide bandwidth required by the FCC for UWB signals [25]. The UWB-OFDM signals are basically a composite of trains of low duty-cycle pulses where each train is modulated by orthogonal sub-carriers. The transmitted signal is of the form

$$X(t) = p(t)e^{j2\pi k f_o t} \quad (3.1)$$

$$p(t) = \sum_{n=0, N-1} s(t - nT)e^{-j2\pi kn/N} \quad (3.2)$$

where $s(t)$ represents the low-pass pulses, such as a Gaussian mono-pulse or a square pulse, $p(t)$ represents the coded pulse train and $k f_o$ the sub-carrier frequency.

$$|P(f)|^2 = |S(f)|^2 \frac{\sin^2(\pi N f T)}{\sin^2(\pi f T)} \quad (3.3)$$

The spectrum of the coded pulse-train is shown in Figure 3.1. It is an over-sampled signal whose spectral peaks occur at frequencies $f = \pm 1/T, \pm 2/T$ and so on. It is obvious that the bandwidth of the main-lobe is $\pm 1/NT$ and the separation between two consecutive main-lobes is $\pm 1/T$.

These signals are best processed in the digital domain and for the most versatile system, the conversion to digital should be done as high up in the receiver chain as possible. The N-Tone $\Sigma\Delta$ converter characteristics perfectly matches the requirements for an N-tone UWB-OFDM signal which can utilize the narrow band-pass and multi-tone property of the signal [26, 1].

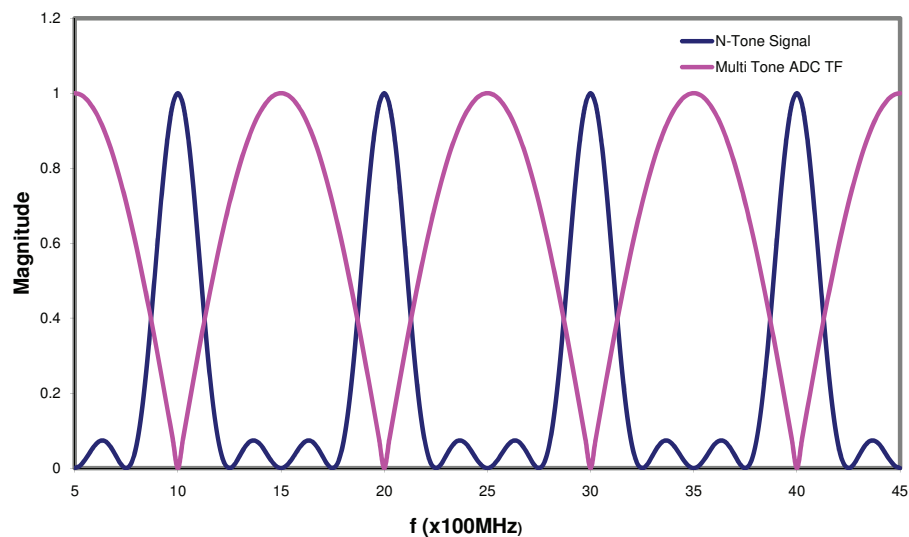


Figure 3.1: Signal/noise spectra for a 4-tone UWB-OFDM

3.2 N-tone $\Sigma\Delta$ Converters

A $\Sigma\Delta$ converter is realized by a loop filter ($H(z)$) and a quantizer (modelled by a variable gain - A_c - and an additive white quantization noise - E_q) in feedback as shown in Figure 3.2. For a low-pass $\Sigma\Delta$ converter the loop filter is an integrator. The signal sees

a low-pass response. But, the quantization noise sees a high-pass response. Thus, quantization noise is effectively shaped away from the signal frequency. Using a resonator in feedback results in a band-pass $\Sigma\Delta$ converter. The in-band signal is faithfully reproduced while quantization noise dominates any out-of-band signal components. Taking this a step further, having a loop-filter with N zeros results in an N -tone $\Sigma\Delta$ Converter.

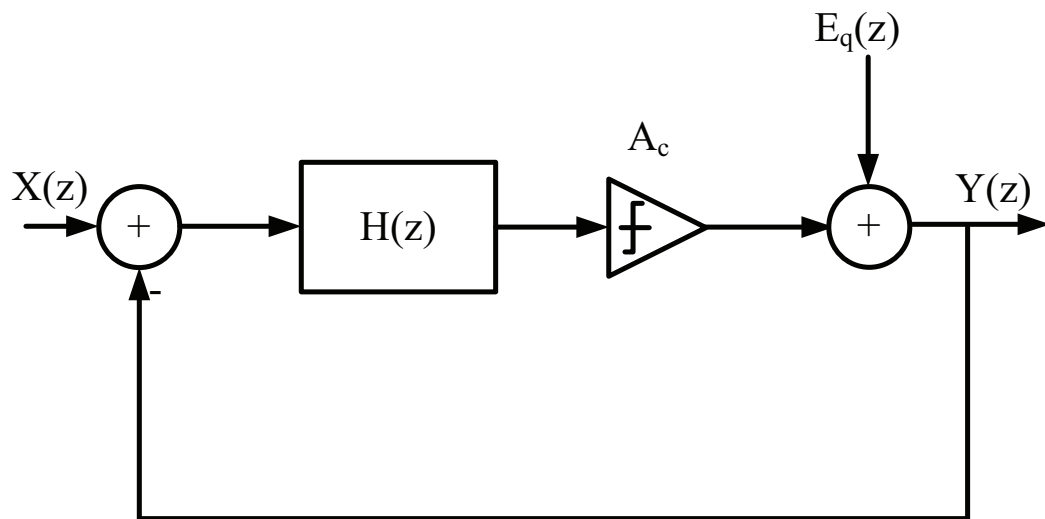


Figure 3.2: Block diagram for a $\Sigma\Delta$ converter

To improve the performance, over-sampling can be employed. Over-sampling is a technique that trades off resolution in time for resolution in amplitude with the use of simple analog components. In a low-pass over-sampled $\Sigma\Delta$ converter, it is imperative that the sampling frequency be much higher than the highest frequency component of the input to obtain a good SNR. But for a band-pass $\Sigma\Delta$ converter, the sampling frequency must just be higher than the bandwidth of the signal. For narrow-band signals,

a very high performance can thus be achieved. This is what makes $\Sigma\Delta$ modulation the architecture of choice for the UWB-OFDM signals. Other techniques normally used to improve the SNR of the converter include the use of higher order loop-filters and multi-bit quantizers. This section focuses on N-tone modulator architectures which employ these techniques.

3.2.1 First Order N-Tone $\Sigma\Delta$ Converter

The simplest and most robust architecture, this has a first order resonator within a feedback loop as shown in Figure 3.3. The comparator is modeled as an additive noise. A detailed analysis follows, which can simply be extended to other architectures too. If $X(z)$ is the input and E_q is the quantization noise, the output can be expressed as

$$Y(z) = X(z) \cdot z^{-2N} + E_q \cdot z^{-2N}(1 + z^{-2N}) \quad (3.4)$$

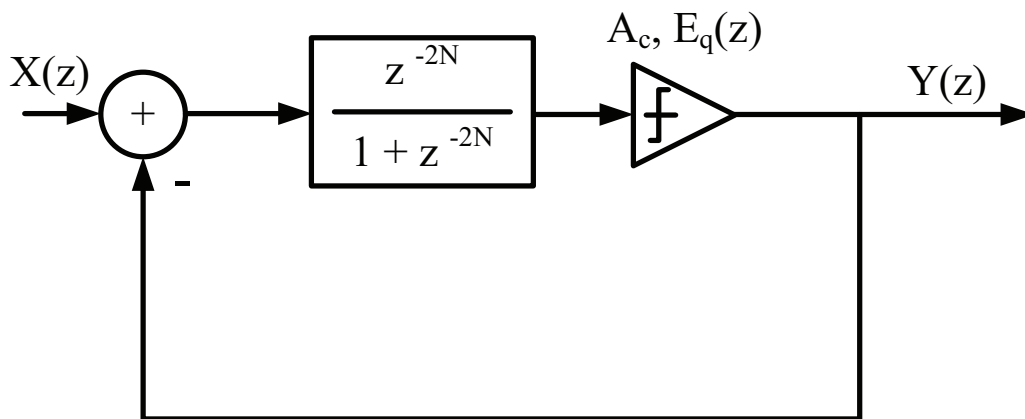


Figure 3.3: Block diagram for a 1st order N-tone $\Sigma\Delta$ converter

The input appears as is after finite delay at the output. But the quantization noise is attenuated at all the NTF zero frequencies. If the sampling frequency is denoted by f_s , the NTF zeros are at

$$f = f_s \frac{(2n + 1)}{4N} \quad \text{where } n = 0, 1, 2 \dots N - 1 \quad (3.5)$$

The output spectrum for a 4-tone $\Sigma\Delta$ modulator with sinusoidal inputs at frequencies $f_s/16, 3f_s/16, 5f_s/16$ and $7f_s/16$ is shown in Figure 3.4. The output spectrum shows the noise valleys which correspond to the input sinusoidal frequencies. Also shown is the input noise floor included in the simulations for dithering.

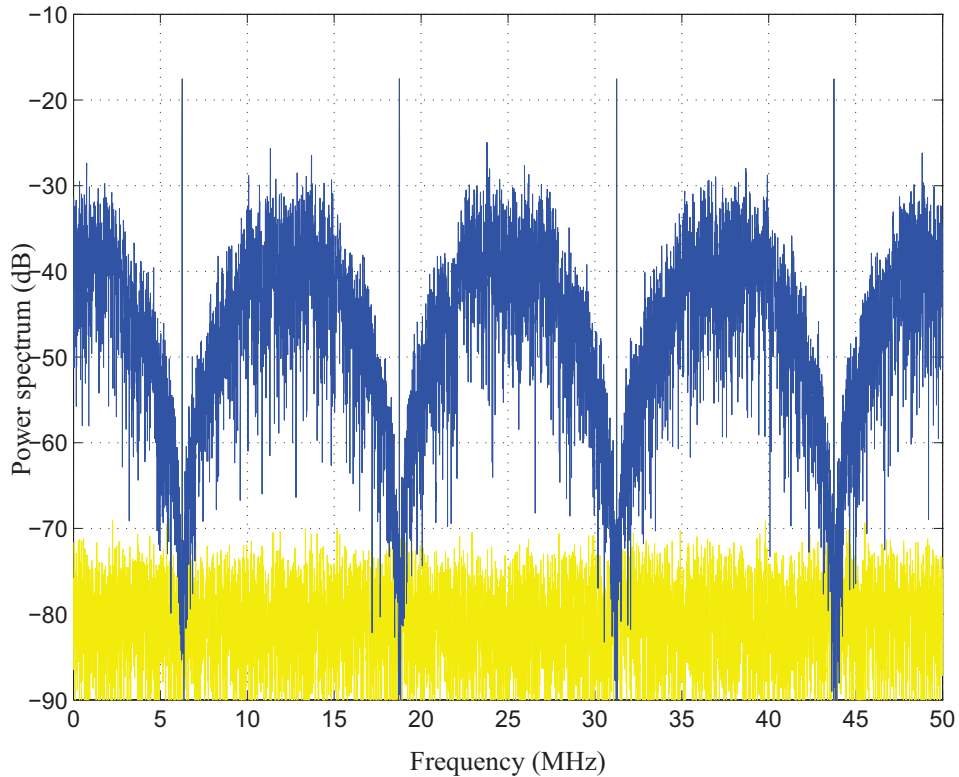


Figure 3.4: Output and input spectra of a 4-Tone $\Sigma\Delta$

It is evident that the spacing between the tones in the N-Tone $\Sigma\Delta$ converter is $2f_s/4N$, where 'N' is the number of tones and f_s is the sampling frequency. The noise-transfer function is given by $N(f)$ -

$$|N(f)|^2 = 4\cos^2(2\pi Nf/f_s) \quad (3.6)$$

The total quantization noise after noise shaping can be calculated as follows. In the equations to follow f_b denotes the signal bandwidth of interest and σ_n refers to the quantization noise power-spectral density.

$$\begin{aligned} P_n &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} |N(f)|^2 \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} 4\cos^2\left(\frac{2\pi Nf}{f_s}\right) \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4\sin^2\left(\frac{2\pi Nf}{f_s}\right) \sigma_n^2 df \\ &\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4\left(\frac{2\pi Nf}{f_s}\right)^2 \sigma_n^2 df \\ &= \frac{\pi^2 N^2 \sigma_n^2}{3 \cdot OSR^3} \end{aligned} \quad (3.7)$$

If the ADC in the $\Sigma\Delta$ converter has a resolution of N_{ADC} . The maximum signal-to-noise ratio(SNR) of this system is given by eqn(3.8).

$$SNR_{max} = 6.02N_{ADC} - 3.4 + 30 \log(OSR) - 20 \log(N) \quad (3.8)$$

where OSR is the over-sampling ratio.

3.2.2 Second Order N-Tone $\Sigma\Delta$ Converter

A second order modulator is shown in Figure 3.5 and is more complex and less robust than the first order modulator. While stability is a concern, the noise-shaping is more pronounced and the resolution of the converter increases more rapidly with OSR as predicted by (3.35).

As in the previous section, the output transfer function is given by Equation 3.9 and the NTF is given by Equation 3.10.

$$Y(z) = X(z) \cdot z^{-2N} + E_q \cdot (1 + z^{-2N})^2 \quad (3.9)$$

$$|N(f)|^2 = 4\cos^2(2\pi N f / f_s) \quad (3.10)$$

$$\begin{aligned} P_n &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} |N(f)|^2 \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} 4\cos^2\left(\frac{2\pi N f}{f_s}\right) \sigma_n^2 df \end{aligned}$$

$$\begin{aligned}
&= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4 \sin^2 \left(\frac{2\pi N f}{f_s} \right) \sigma_n^2 df \\
&\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4 \left(\frac{2\pi N f}{f_s} \right)^2 \sigma_n^2 df \\
&= \frac{\pi^2 N^2 \sigma_n^2}{3 \cdot OSR^3} \tag{3.11}
\end{aligned}$$

The maximum achievable SNR for the system is given by

$$SNR_{max} = -5.1 + 50 \log(OSR) - 40 \log(N) \tag{3.12}$$

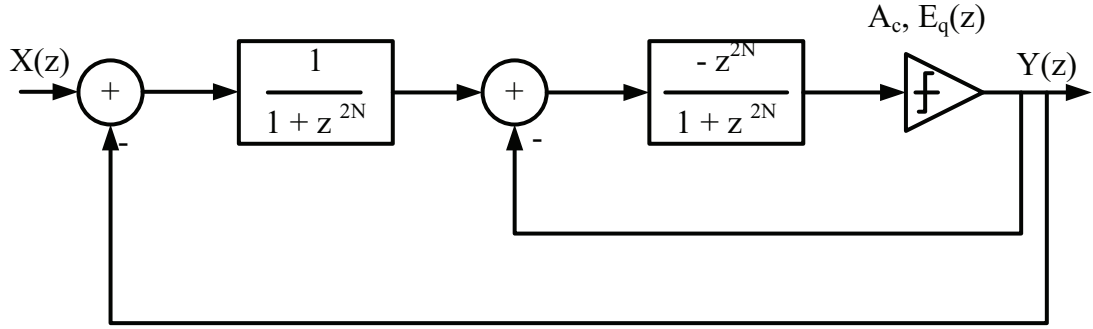


Figure 3.5: Block diagram for a 2nd order N-tone $\Sigma\Delta$ converter

3.2.3 L-th Order N-Tone $\Sigma\Delta$ Converter

In general, for an L-th order modulator (Figure 3.6), the noise power and maximum achievable SNR are given by Equation 3.15. Higher order systems are more prone to

instability.

$$P_n = \pi^{2L} N^{2L} \sigma_n^2 / (2L + 1) OSR^{2L+1} \quad (3.13)$$

$$|N(f)|^2 = 4 \cos^2(2\pi N f / f_s) \quad (3.14)$$

$$\begin{aligned} P_n &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} |N(f)|^2 \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} 4 \cos^2\left(\frac{2\pi N f}{f_s}\right) \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4 \sin^2\left(\frac{2\pi N f}{f_s}\right) \sigma_n^2 df \\ &\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 4 \left(\frac{2\pi N f}{f_s}\right)^2 \sigma_n^2 df \\ &= \frac{\pi^2 N^2 \sigma_n^2}{3 \cdot OSR^3} \end{aligned} \quad (3.15)$$

$$SNR_{max} = 7.8 - 20 \cdot L \log(\pi N) + 10 \cdot \log((2L + 1) OSR^{2L+1}) \quad (3.16)$$

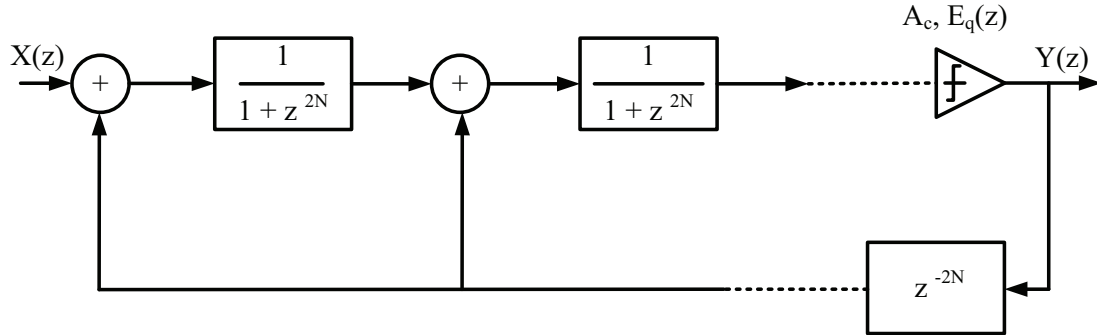


Figure 3.6: Block Diagram of an L-th order N-tone $\Sigma\Delta$ converter

3.2.4 Multi-bit N-Tone $\Sigma\Delta$ Converter

Besides using over-sampling and higher-order noise-shaping functions, we can also use a multi-bit ($N_{sub-ADC}$) quantizer to improve the maximum achievable SNR.

$$SNR_{max} = 6.02N_{sub-ADC} + 1.76 - 20L \cdot \log(\pi N) + 10 \cdot \log[(2L+1) \cdot OSR^{(2L+1)}] \quad (3.17)$$

However, the use of a multi-bit quantizer places stringent requirements on the DAC linearity and any deviation from the ideal DAC levels can result in distortion. To avoid this, we can employ tricks that are used in low-pass implementations such as multi-bit quantizers with a single-bit feedback [27].

3.3 Cascaded Higher Order N-Tone $\Sigma\Delta$ Converters

Shown in Figure 3.7 is the block diagram of the generalized two-stage Cascaded N-tone $\Sigma\Delta$ converter. As seen in the figure, the quantization noise of the first stage forms the input to the second stage. The second stage thus senses the quantization

noise introduced by the first-stage quantizer and the “Digital Error Correction” block compensates for the noise-shaping of $E_q(z)$ in first stage and cancels it out. Thus, only the quantization noise of the second stage appears at the output. And, as this sees the noise shaping of both the stages, the SNR of the overall system is improved and resembles that of a second-order $\Sigma\Delta$ Converter. However, the system does not suffer from instability issues of the same.

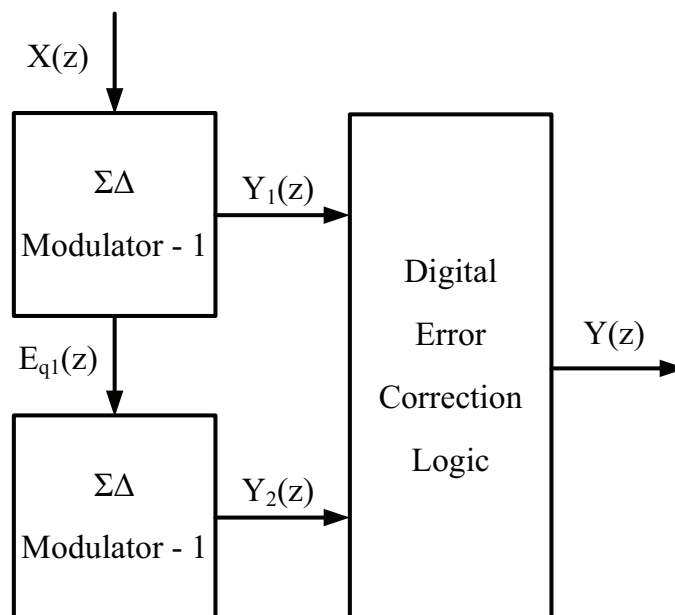


Figure 3.7: Block diagram for a Cascaded N-tone $\Sigma\Delta$

Let $H_1(z)$ and $N_1(z)$ be the STF and NTF of the first stage, then

$$Y_1(z) = X(z) \cdot H_1(z) + E_q(z) \cdot N_1(z) \quad (3.18)$$

Similarly, let $H_2(z)$ and $N_2(z)$ be the STF and NTF of the second stage, then

$$Y_2(z) = E_q(z) \cdot H_2(z) + E_{q2}(z) \cdot N_2(z) \quad (3.19)$$

where $E_{q2}(z)$ is the quantization noise of the second stage. After the digital error correction,

$$Y(z) = Y_1(z) \cdot H_2^*(z) - Y_2(z) \cdot N_1^*(z) \quad (3.20)$$

$$Y(z) = X(z) \cdot H_1(z) \cdot H_2(z) - E_{q2}(z) \cdot N_2(z) \cdot N_1(z) \quad (3.21)$$

Thus, the overall NTF, is the product of the NTFs of the cascaded stages. The effective NTF of 'n' stages in cascade is

$$N(z) = N_1(z) \cdot N_2(z) \cdots N_n(z) \quad (3.22)$$

As predicted, the quantization noise of the first stage is canceled completely only if the digital estimations - $H_2^*(z)$ and $N_1^*(z)$ - are equal to the actual values of the STF and NTF - $H_2(z)$ and $N_1(z)$. Mismatches between the estimates and actual values result in imperfect cancelation of noise from the first stage and deteriorates SNR. Thus, the number of stages that can practically be cascaded together is limited only by the precision of the digital error correction.

3.3.1 Cascaded N-2N Tone $\Sigma\Delta$ Converter

If the second stage introduces zeros in the NTF at $f_s/4N$, the noise-performance could be improved by placing zeros at the edge of the signal-band where the in-band noise is at its maximum. The easiest way of implementing this, if the signal bandwidth was $f_s/8N$ would be to cascade an N-Tone and a 2N-Tone $\Sigma\Delta$ Converter as shown in Figure 3.8. Noting that this is nothing but a cascade of an N-Tone and 2N-Tone, the transfer function can be readily found to be (3.29) [28].

$$N(z) = N_1(z) \cdot N_2(z) \quad (3.23)$$

where

$$N_1(z) = (1 + z^{-2N}) \quad (3.24)$$

$$N_2(z) = (1 + z^{-4N}) \quad (3.25)$$

$$H(z) = H_1(z) \cdot H_2(z) \quad (3.26)$$

where

$$H_1(z) = -z^{-2N} \quad (3.27)$$

$$H_2(z) = -z^{-4N} \quad (3.28)$$

$$Y(z) = X(z) \cdot z^{-6N} + E_{q2}(z) \cdot (1 + z^{-2N}) \cdot (1 + z^{-4N}) \quad (3.29)$$

The total quantization noise after noise shaping can be calculated as follows:

$$|N(f)|^2 = 16 \cos^2 \left(\frac{2\pi N f}{f_s} \right) \cos^2 \left(\frac{4\pi N f}{f_s} \right) \quad (3.30)$$

$$\begin{aligned} P_n &= \frac{2}{f_s} \int_{(2n+1)f_s/4N - f_b/2}^{(2n+1)f_s/4N + f_b/2} |N(f)|^2 \sigma_n^2 df \\ &= \frac{16}{f_s} \int_{(2n+1)f_s/4N - f_b/2}^{(2n+1)f_s/4N + f_b/2} 16C(f) \sigma_n^2 df \end{aligned}$$

$$\text{where, } C(f) = \cos^2 \left(\frac{2\pi N f}{f_s} \right) \cos^2 \left(\frac{4\pi N f}{f_s} \right)$$

$$\begin{aligned}
&= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 16 \sin^2 \left(\frac{2\pi N f}{f_s} \right) \cos^2 \left(\frac{4\pi N f}{f_s} \right) \sigma_n^2 df \\
&\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 16 \left(\frac{2\pi N f}{f_s} \right)^2 \sigma_n^2 df \tag{3.31}
\end{aligned}$$

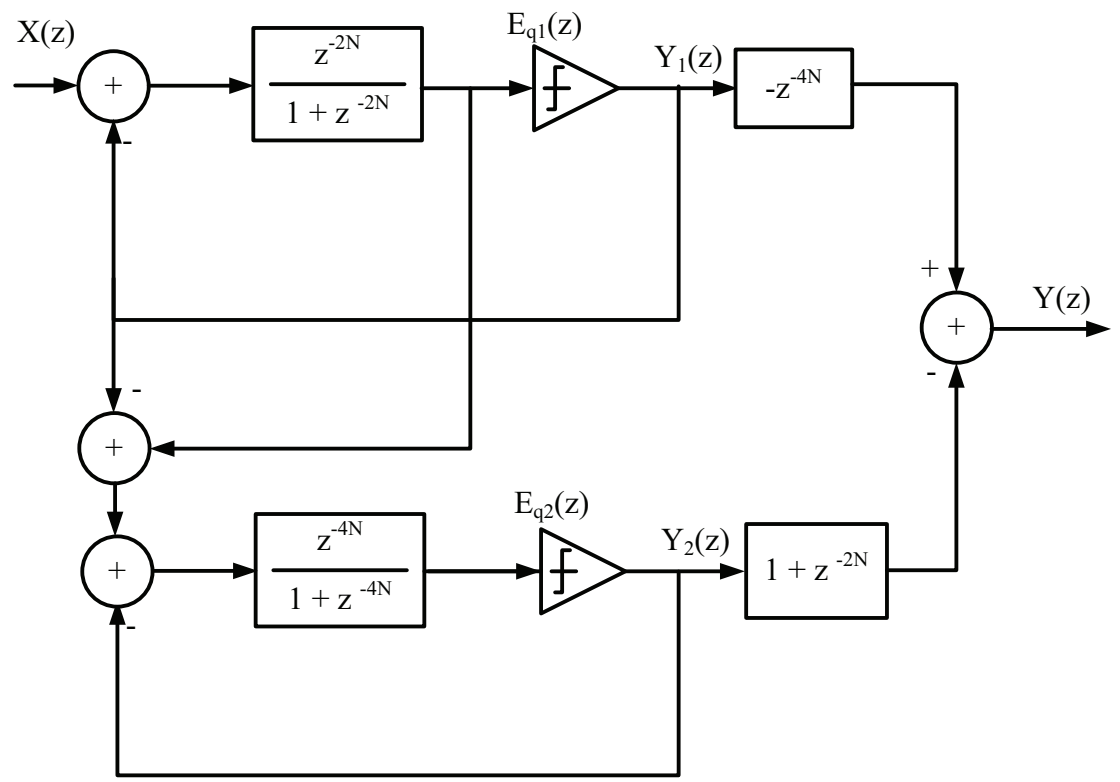


Figure 3.8: Block diagram for a Cascaded N-2N Tone $\Sigma\Delta$ with noise-shaping

As can be seen, for high over-sampling ratios, this architecture provides performance similar to that of a first order N-Tone $\Sigma\Delta$ converter. This is because at high over-sampling ratios, the zeros introduced by the 2N-Tone stage do not shape the in-band

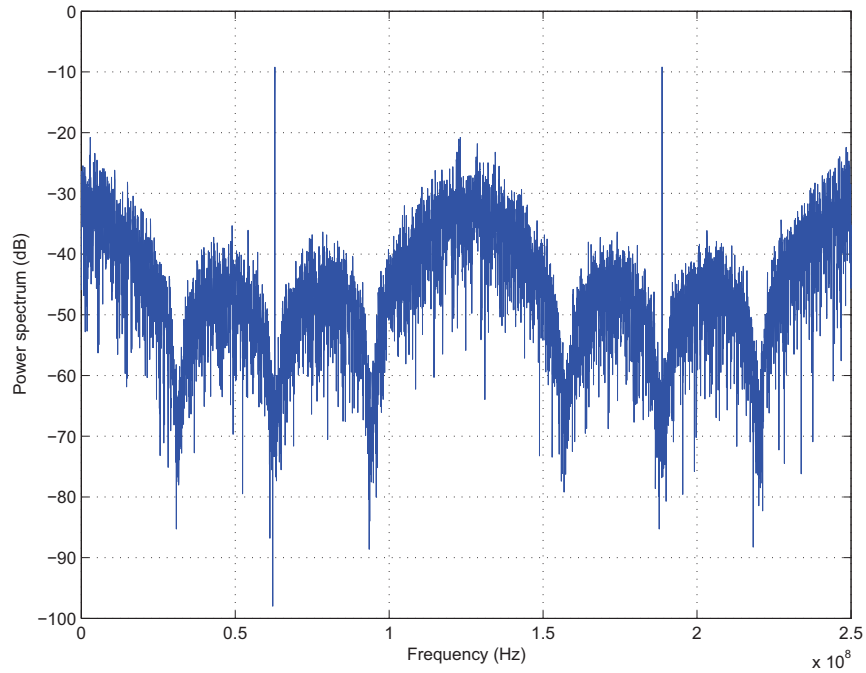


Figure 3.9: Output spectrum of a Cascaded N-2N tone $\Sigma\Delta$ with noise-shaping noise. When we have over-sampling ratios such that the zeros introduced by the 2N-tone stage are at desired signal band-edge, we see a considerable improvement in SNR as compared to a first order $\Sigma\Delta$ converter.

As shown in Figure 3.9 the overall transfer function is a product of the NTFs of an N-Tone $\Sigma\Delta$ and a 2N-Tone $\Sigma\Delta$. With an over-sampling ratio of 16, simulations of the behavioral model in SIMULINK, shows the SNR achieved for a Cascaded N-2N Tone $\Sigma\Delta$ Converter to be about 24dB.

3.3.2 MASH N-Tone $\Sigma\Delta$ Converter

A special case of the cascaded $\Sigma\Delta$ Converter, is the MASH implementation for N-tone $\Sigma\Delta$ converter [29, 13, 30]. It has in cascade two lower order N-Tone $\Sigma\Delta$ Converters. Their outputs summed in such a way that the quantization noise of the first modulator is canceled (under ideal conditions) while the quantization noise of the second modulator sees a higher order shaping. This combines the higher-order noise-shaping with the robustness of the lower order modulator. Figure 3.10 shows the second order MASH-counterpart for the N-tone $\Sigma\Delta$ converter [31]. The transfer function is given by Equation 3.32 and the SNR is similar to that of a second-order modulator (Eqn 3.35).

$$Y(z) = X(z) \cdot z^{-2N} + E_q(z) \cdot (1 + z^{-2N})^2 \quad (3.32)$$

$$|N(f)|^2 = 16\cos^4(2\pi Nf/f_s) \quad (3.33)$$

$$\begin{aligned} P_n &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} |(N(f)|^2 \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{(2n+1)f_s/4N-f_b/2}^{(2n+1)f_s/4N+f_b/2} 16\cos^4\left(\frac{2\pi Nf}{f_s}\right) \sigma_n^2 df \\ &= \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 16\sin^4\left(\frac{2\pi Nf}{f_s}\right) \sigma_n^2 df \\ &\approx \frac{2}{f_s} \int_{-f_b/2}^{+f_b/2} 16\left(\frac{2\pi Nf}{f_s}\right)^4 \sigma_n^2 df \end{aligned}$$

$$= \frac{\pi^4 N^4 \sigma_n^2}{9OSR^5} \quad (3.34)$$

$$SNR_{max} = -5.1 + 50 \log(OSR) - 40 \log(N) \quad (3.35)$$

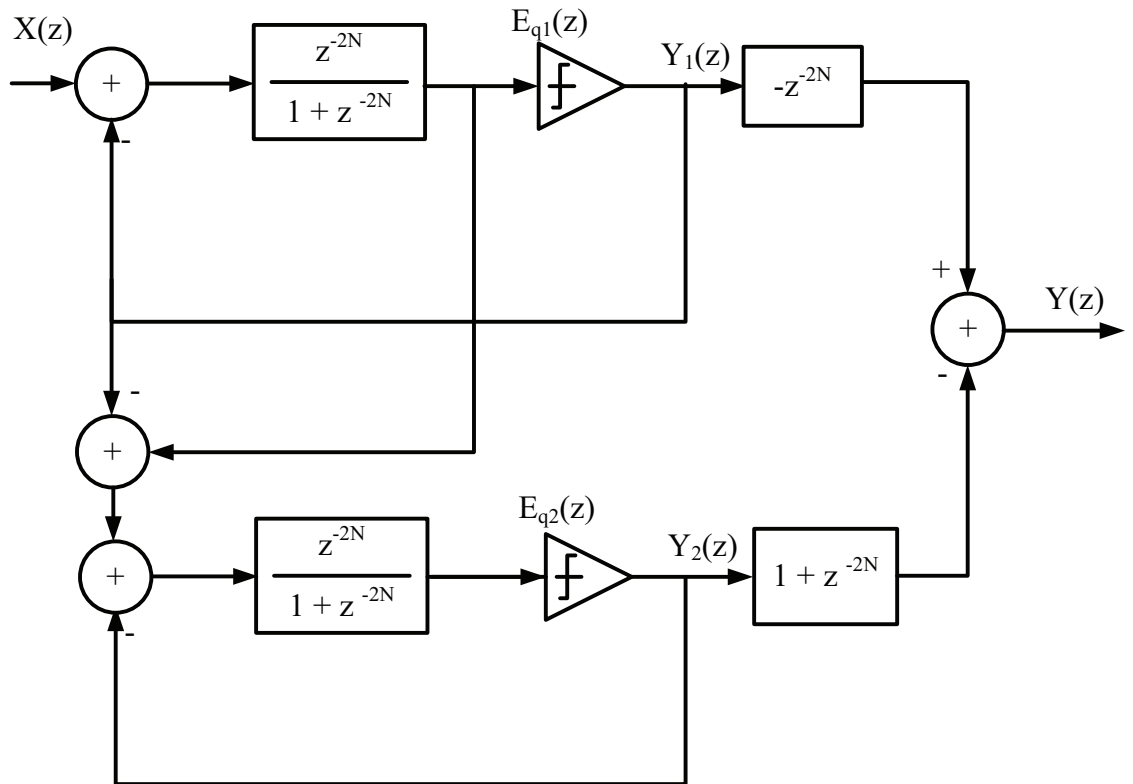


Figure 3.10: Block diagram for a MASH implementation of a N-tone $\Sigma\Delta$

With an over-sampling ratio of 16, simulations of the behavioral model in SIMULINK, shows the SNR achieved for a second-order MASH to be about 34dB (Figure 3.11).

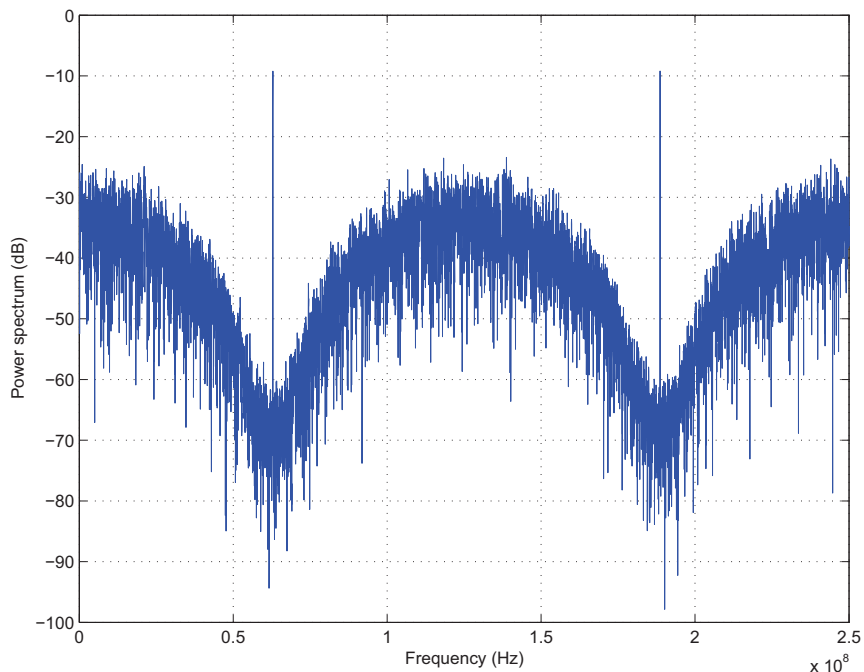


Figure 3.11: Output spectrum of a II order MASH N-tone $\Sigma\Delta$

3.3.3 Optimal Placement of Zeros of the NTF

It is worthwhile to look at the variation of SNR with over-sampling ratio as in Figure 3.12. In other words - the variation of SNR for a fixed NTF as the signal bandwidth is varied. For high over-sampling ratio, the second-order MASH architecture is better than the Cascaded N-2N Tone architecture by atleast 12dB. This is not surprising, simply because the former has a two zeros at $f_s/4N$ while the latter has a single zero at $f_s/4N$. However, as over-sampling ratio reduces, the zero introduced by the 2N-Tone $\Sigma\Delta$ converter starts attenuating noise in the signal-band and the two performances become comparable. In fact, at over-sampling ratio of about 1.5, the Cascaded N-2N tone $\Sigma\Delta$ converter has about 6dB better SNR. This can be attributed to the fact that,

for an over-sampling ratio of 1.5, the NTF zeros are *optimally* placed.

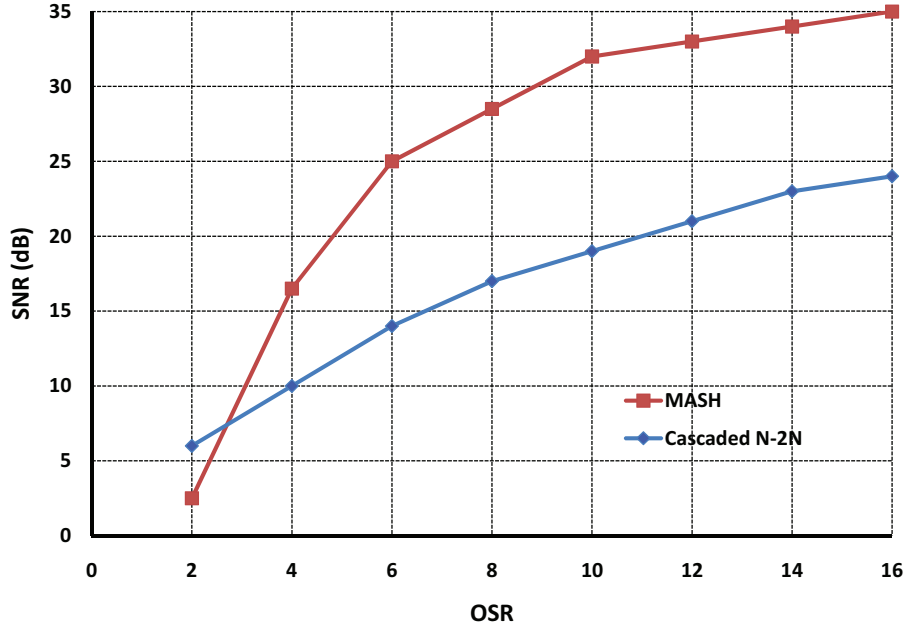


Figure 3.12: SNR vs. OSR for the MASH and Cascaded N-2N Tone $\Sigma\Delta$ with noise-shaping

It is a well-known fact that if the zeros in the NTF are spread across the desired band, the in-band noise power can be reduced. Generally, using the largest number of complex zero pairs would result in best possible noise-shaping. However, the optimal solution in terms of total integrated noise in the desired band has been analytically determined [32]. Citing those results, for a system with three zeros, the optimal zero locations turn out to be

$$\omega_z = [0, \pm \text{sqrt}(3/5)] \cdot \omega_B \tag{3.36}$$

where ω_B is the signal bandwidth. This explains why the SNR of the cascaded N-2N

Tone $\Sigma\Delta$ converter peaks for over-sampling ratio of 1.5. The SNR, however, at this point is intolerably low due to the extremely low over-sampling ratio. An alternate solution would be to use the interpolative $\Sigma\Delta$ converter [33] instead of the 2N-Tone $\Sigma\Delta$ converter, to specifically place the zeros at the optimal locations depending on the signal band-width.

3.4 Non-idealities in an N-Tone $\Sigma\Delta$ Converter

In all the above calculations for maximum achievable SNR, the resonator is assumed to be lossless. But, when the loop-filter is implemented by a switched-capacitor N-path filter, finite DC-gain, bandwidth and slewing constraints in the op-amp result in a lossy loop-filter. Leakage of charge in such a filter results in non-infinite attenuation of noise at the desired notch frequency. This increases the noise floor and reduces the SNR [34]. This could also be visualized as an undesired movement in the notch frequency. Other causes for SNR degradation would be the thermal noise from the capacitors and amplifiers, and mismatches in the resonator capacitors.

To get a basic understanding of how these noise sources contribute to the overall system noise, let us also include E_c - the input referred noise at the comparator along with the quantization noise [35]. With a comparator gain of A_c as in Figure 3.13, the transfer function of the modulator is given by

$$Y(z) = \frac{X(z)A_cHz^{-2N}}{1 - A_cHz^{-2N}} + \frac{E_cA_cz^{-2N}}{1 - A_cHz^{-2N}} + \frac{E_qz^{-2N}}{1 - A_cHz^{-2N}} \quad (3.37)$$

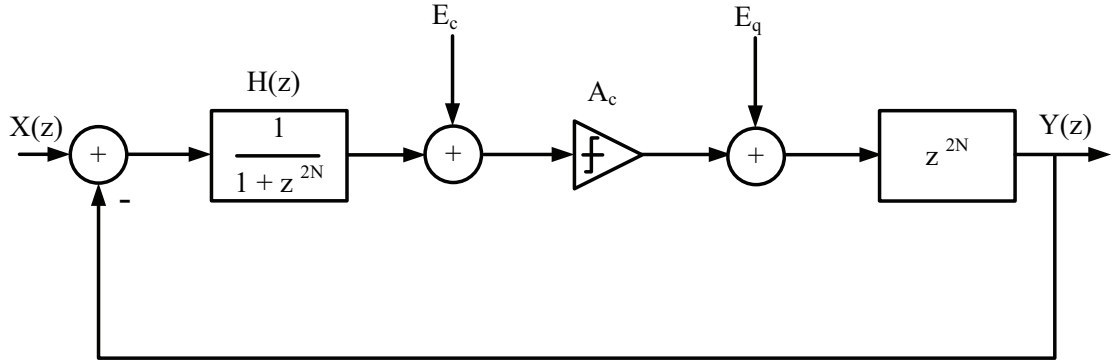


Figure 3.13: Block diagram for an N-tone $\Sigma\Delta$ converter with noise sources

$$Y(z) \approx \left(X(z) + \frac{E_c}{H} + \frac{E_q}{A_c H} \right) \quad (3.38)$$

The approximation is valid for high loop-gains at the notch frequencies. It is evident that while quantization noise is attenuated by the gain of the comparator at the input of the modulator, the comparator noise appears directly. This implies that the comparator used in this implementation should have high resolution and low noise. Also, any noise that gets added after the loop-filter will be shaped but any noise at the input of the system will not be shaped by the loop-filter. Having mentioned this, we now look at the various sources of non-idealities.

3.4.1 Jitter in the sampling clock

Since the N-Tone $\Sigma\Delta$ converter is a sampled system, the variations in the clock period have no effect on the system once the input has been sampled. However, jitter on the

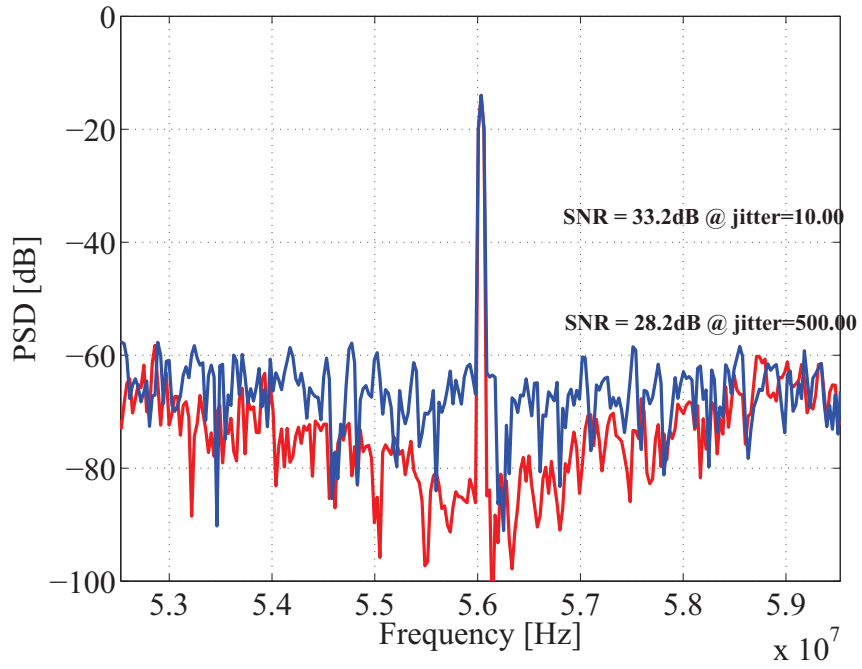


Figure 3.14: Effect of jitter on the output spectrum

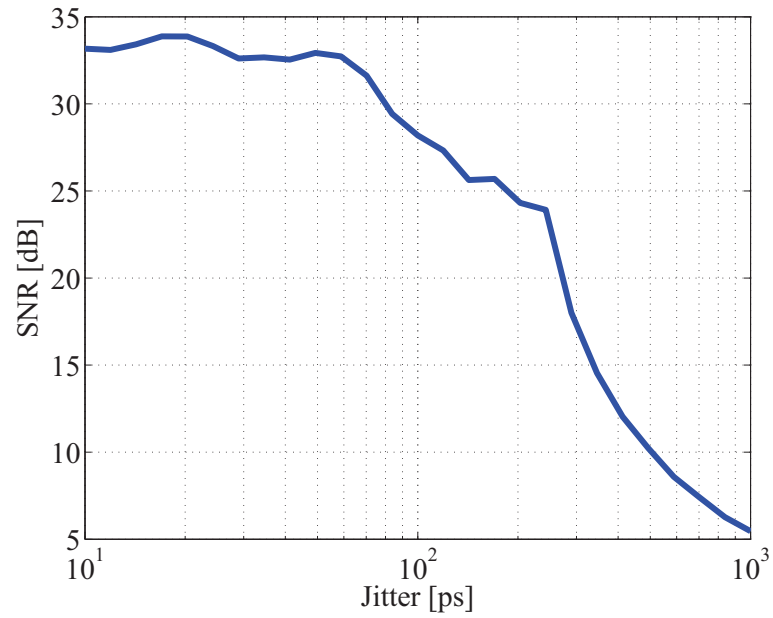


Figure 3.15: Effect of jitter on the output spectrum

clock affects the input sampled by the system. The error in the sampled signal is given by

$$\Delta x = 2\pi f_{in} A \delta \cos(2\pi f_{in} t) \quad (3.39)$$

where A is the signal magnitude, f_{in} is the signal frequency and δ is the instantaneous jitter on the clock. Given that the jitter can be considered to be a random process with a standard deviation of σ_t , the power of the error signal is given by [36]

$$S_{\Delta} = \frac{(2\pi f_{in} A \sigma_t)^2}{2} \quad (3.40)$$

Since this appears at the input, it is not shaped away (Figure 3.14) but instead is reduced by the over-sampling ratio if the jitter is white. And, as is obvious, it is the input at the N^{th} tone that is most affected by jitter by a factor of $10 \cdot \log_{10}(N)$. (Figure 3.15).

3.4.2 Thermal noise from capacitors and amplifiers

The thermal noise due to sampling of the switch noise on the input sampling capacitors, hold-phase capacitors and the amplifier thermal noise can all be combined into one equivalent noise source at the input. As it appears in the signal path, it does not see the noise shaping and like jitter is reduced only by a factor of over-sampling as can be seen in Figure 3.16. The total noise power at the input can be quantified as

$$S_{thermal} = V_{n,amp}^2 + \frac{kT}{C_s} + \frac{kT}{C_h} \cdot \left(\frac{F}{G}\right)^2 \quad (3.41)$$

where $V_{n,amp}$ is the input referred noise of the amplifier used in the resonator, C_s is the sampling capacitor, C_h is the hold-phase capacitor, G is the gain in the resonator and

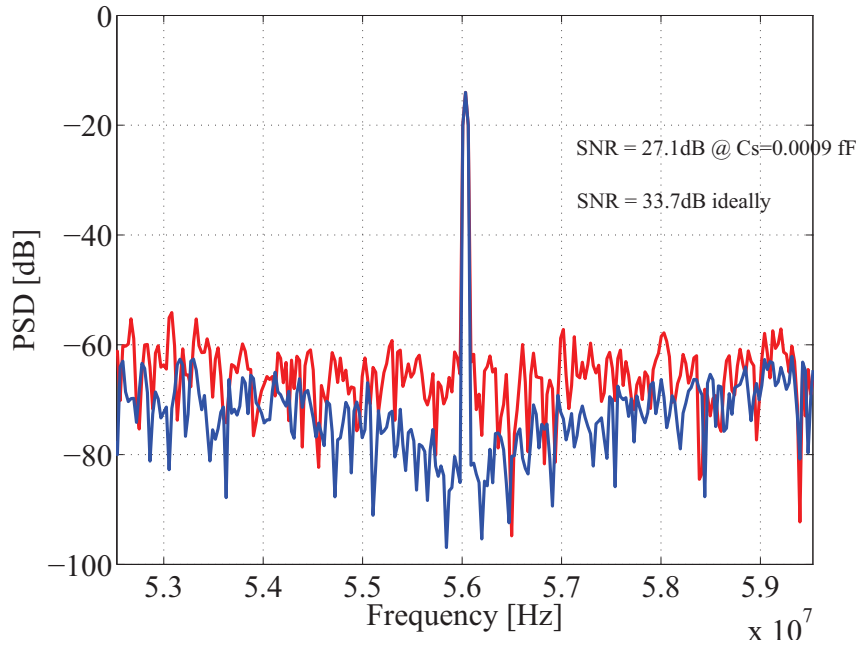


Figure 3.16: Effect of kT/C noise on the output spectrum

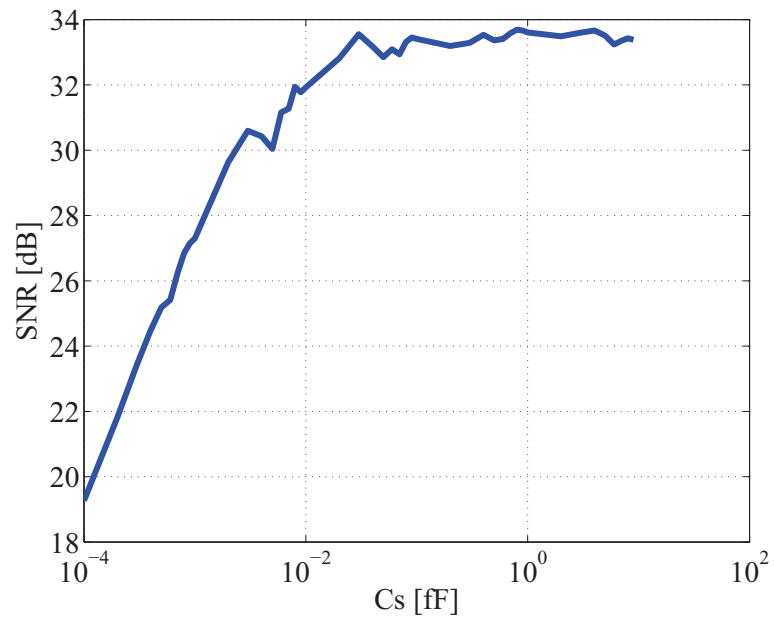


Figure 3.17: Effect of kT/C noise on the SNR

F is the form-factor. Thus, the kT/C noise only increases the noise floor which reduces SNR. It does not introduce tones or harmonics. Shown in Figure 3.17 is the degradation of SNR with thermal noise (x-axis represents the equivalent noise capacitance and is specified in femto Farads). The maximum expected SNR without any noise is 33.75dB.

3.4.3 Finite gain and settling in the amplifier

When the amplifier used in the resonator has finite DC gain and bandwidth, it means that instead of subtracting $y[n-2N]$ from the $y[n]$, we are in fact subtracting only $\alpha \cdot y[n - 2N]$ (α takes into account DC gain error). This implies that the resonator is lossy(3.42), resulting in a degradation of SNR. Simulations for finite gain impact are seen in Figures 3.18,3.19. As gain reduces the output becomes tonal since the assumption of white quantization noise no longer holds. The effect of finite slew-rate and bandwidth can be considered as the effect of non-linear gain. This not only degrades the SNR but also introduces harmonic distortion as seen in Figures 3.20-3.23. It is to be noted that finite UGB does not deteriorate the SNR as long as the amplifier is not slew-rate limited.

$$\frac{Y(z)}{X(z)} = \frac{\beta}{1 + \alpha z^{-2N}} \quad (3.42)$$

3.4.4 Mismatch in resonator capacitors

Mismatch among the individual capacitors, however, is much more problematic. The very first effect is that it varies the coefficients of the resonators, which will result in

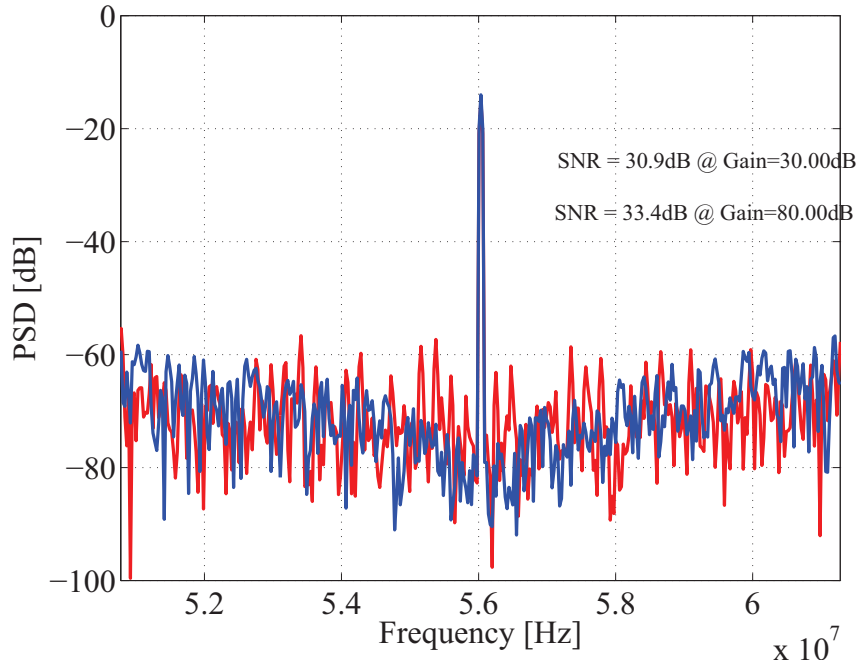


Figure 3.18: Effect of amplifier gain on the output spectrum

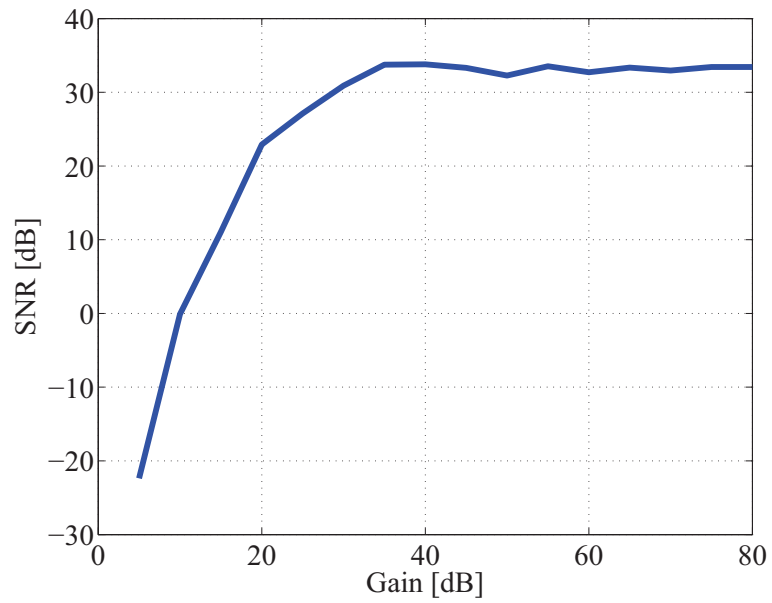


Figure 3.19: Effect of amplifier gain on the SNR

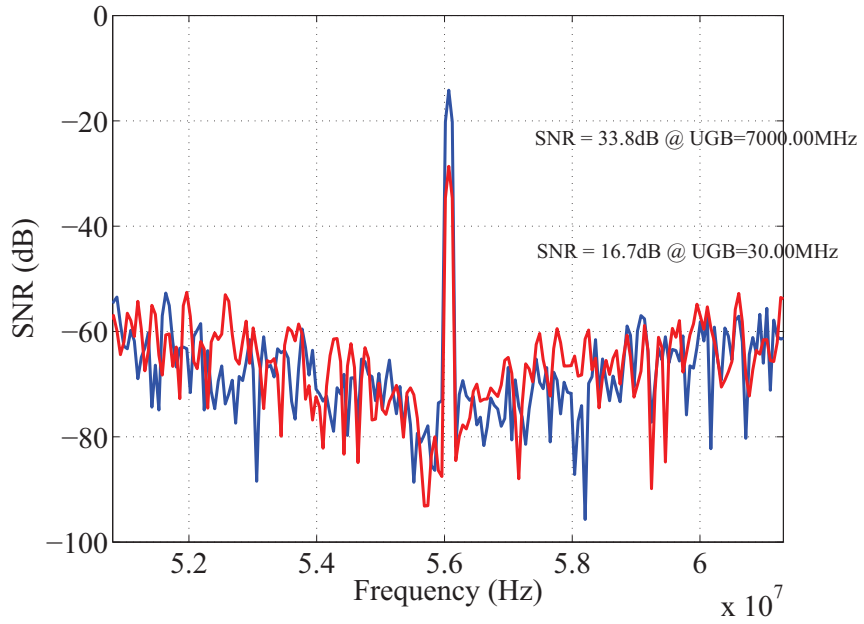


Figure 3.20: Effect of amplifier UGB on the output spectrum

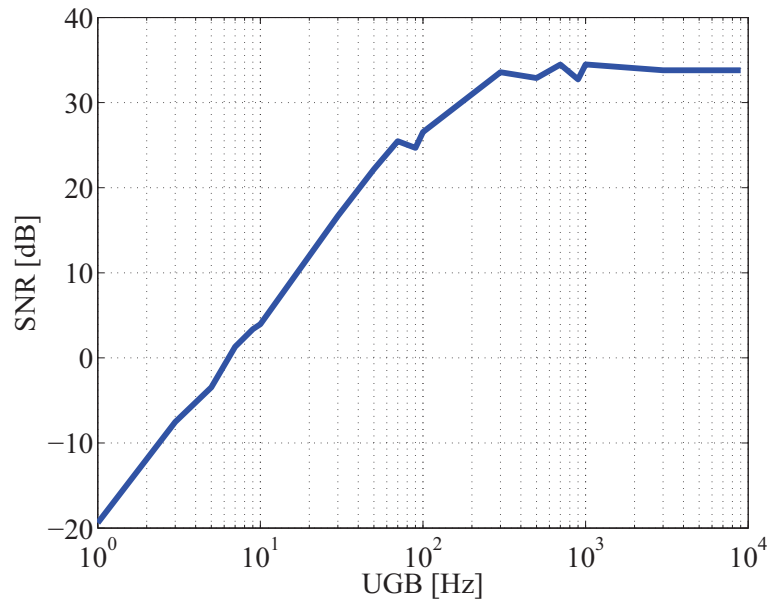


Figure 3.21: Effect of amplifier UGB on the SNR

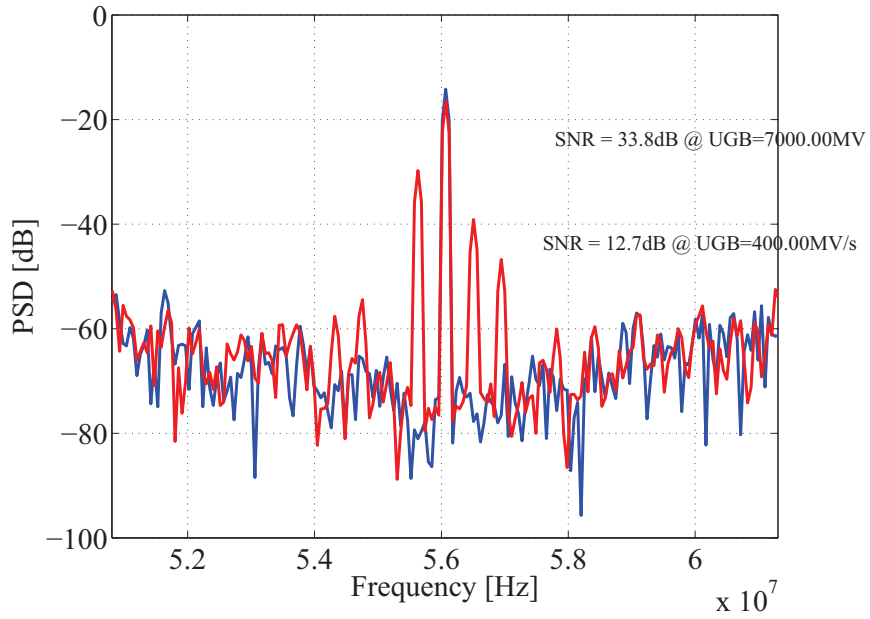


Figure 3.22: Effect of amplifier slew-rate on the output spectrum

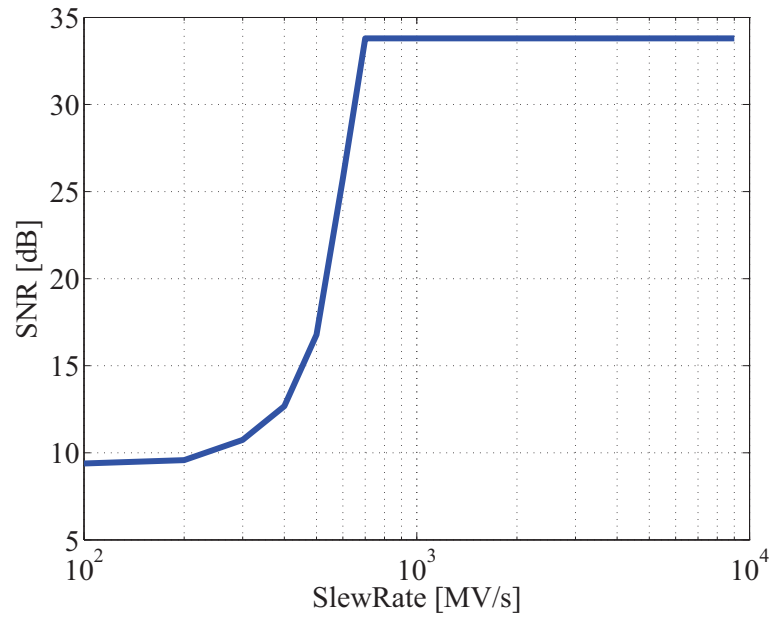


Figure 3.23: Effect of amplifier slew-rate on the SNR

the movement of the zeros of the NTF away from the desired frequency. This shows up as a loss in SNR. Additionally, this results in the coefficients varying periodically with a frequency of f_s/N , which introduces harmonics (as seen in Figure 3.24) and spectral leakage from the other notch frequencies. Figure 3.25 shows the variation of SNR with mismatch. For the OSR and design selected there is about a 3dB reduction in SNR for $\pm 5\%$ mismatch. The impact would be significantly more severe if a higher performance design were desired.

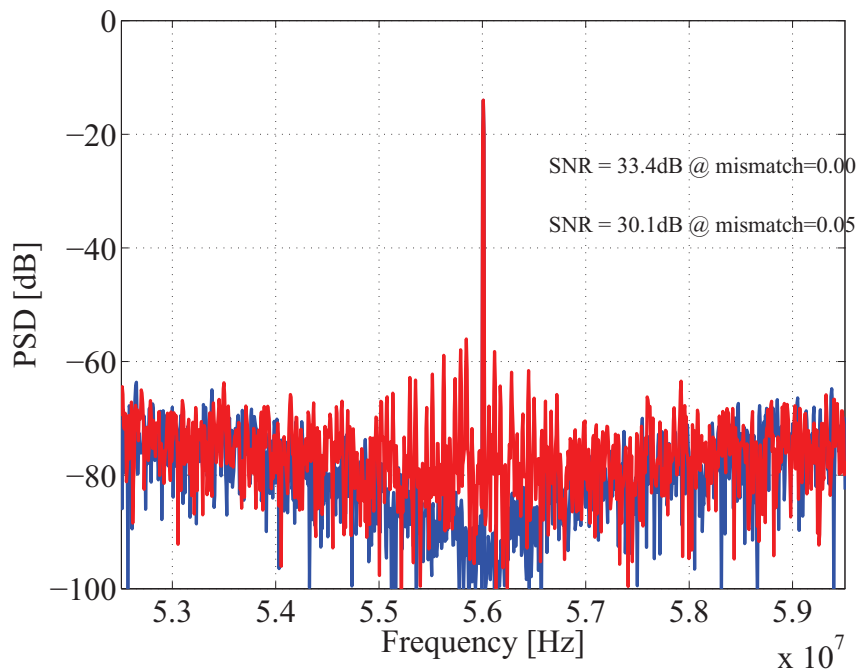


Figure 3.24: Effect of mismatch on the output spectrum

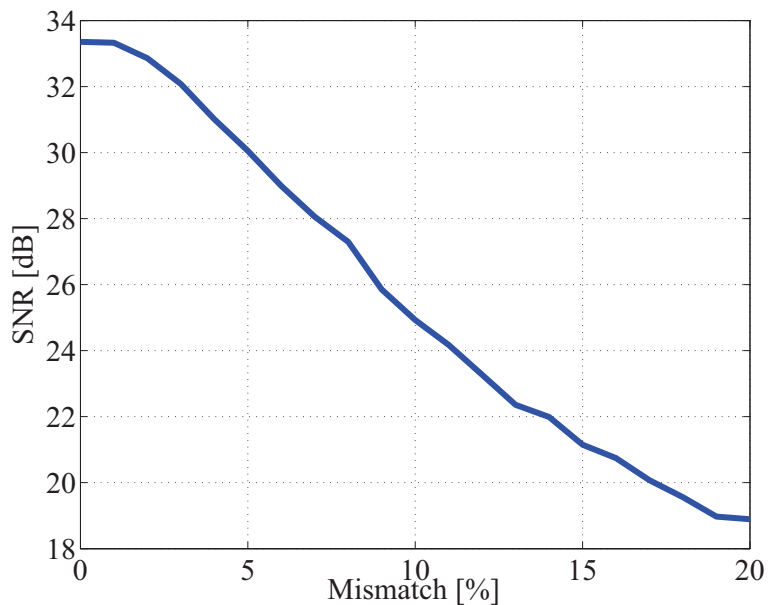


Figure 3.25: Effect of mismatch on the SNR

3.5 Circuit Implementations

3.5.1 Low-power Implementation

Usually, the loop-filter is implemented as a switched-capacitor, switched-current or continuous-time filter. Among all the components in such an active $\Sigma\Delta$ converter, the operational amplifiers in the integrators/resonators consume the maximum power [35]. It is obvious that replacing the active loop filter by a passive one would result in tremendous reduction in power consumption. The passive filter, however, would have no gain. The large loop gain needed to suppress the quantization noise will now have to be provided by the comparator. With the result that a multi-bit quantizer cannot be used

for such a passive converter. Though a passive implementation of an N-tone $\Sigma\Delta$ converter would be attractive in terms of power, it has additional limitations which will be discussed shortly.

When the resonator is implemented through charge-sharing between capacitors, as in [35], it always results in a leaky resonator because the charge finally transferred from the sampling capacitor is always a fraction of the input charge and never the total input charge. To circumvent this problem, we use a scheme like the inverter-based design for the charge-transfer mechanism [37]. The switched-capacitor based integrator is lossless owing to the fact that the virtual ground at the hold-phase switch ensures that the voltage on the non-input end of the C_s does not change. Maintaining the non-input end of C_s at a constant value can be accomplished in the passive implementation by having a buffer as shown in Figure 3.26. The input is sampled with reference to the output. This results in a charge of $C_s(y[n-1] - x[n])$ across C_s . The charge on the integrating capacitor is $C_h(y[n-1])$. When the sampling capacitor is connected across the integrating capacitor during the hold phase, the charge in the system is $(C_s + C_h)y[n]$. From conservation of charge,

$$y[n] = y[n-1] + \frac{C_s}{(C_s + C_h)}x[n] \quad (3.43)$$

The deterioration in SNR due to the non-ideal behavior of the buffer - gain errors and settling errors - dictate the minimum gain and bandwidth requirements of the buffer. These errors should effectively be less than the accuracy of the entire system. Figure 3.19 shows that for a low SNR, a very high gain in the buffer is not necessary.

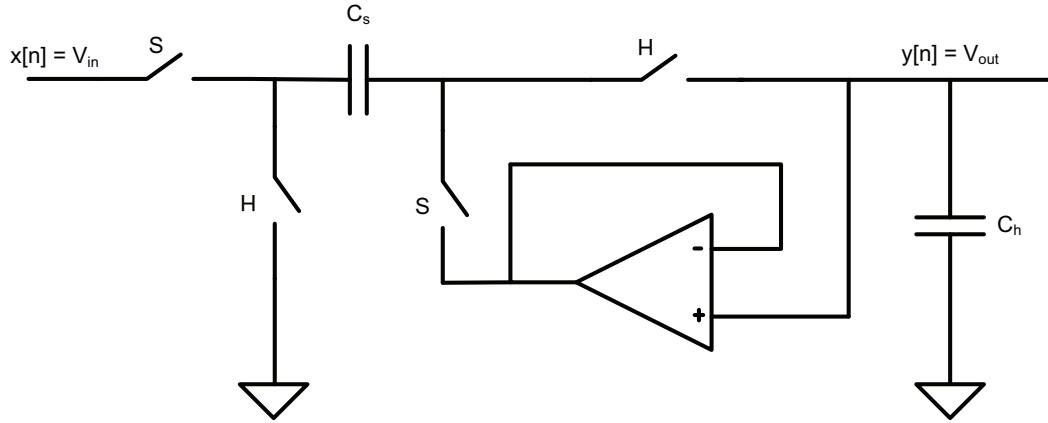


Figure 3.26: Lossless Integrator

Figure 3.27 shows a single-ended version of a 2-Tone $\Sigma\Delta$ converter based on the buffer scheme described above. C_s acts as the sampling capacitor. In the ideal case, having a buffer between the output to the sampling capacitor enables us to obtain a lossless loop filter. Here, $C_{a,b..d}$ are the storage capacitors. The outputs are stored consecutively on C_a C_b C_c and then C_d . After cycling through all the storage capacitors once, it is time to retrieve the stored value from the capacitor and subtract it from the input. This is accomplished by flipping the storage capacitors. The clocking scheme is as depicted in Figure 3.28. The equations that govern the switched-capacitor filter are given in the following equations.

$$C_s \cdot (-y[n - 4] - x[n]) - C_a y[n - 4] = (C_s + C_a) \cdot y[n] \quad (3.44)$$

$$y[n] + y[n - 4] = -x[n] \cdot C_s / (C_s + C_a) \quad (3.45)$$

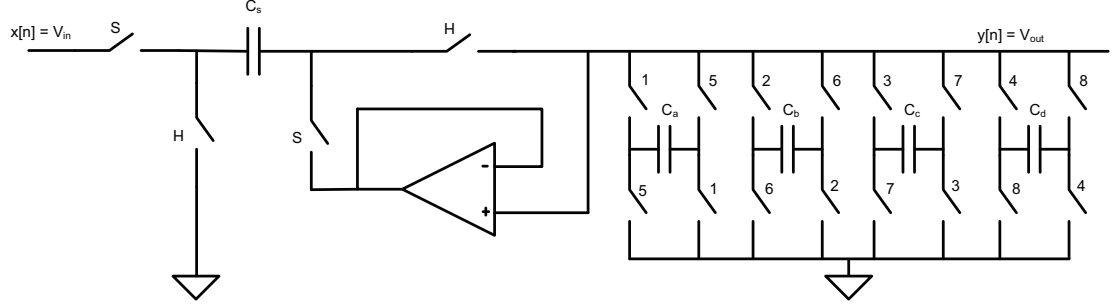


Figure 3.27: Single-ended implementation of the 2-Tone $\Sigma\Delta$ converter

$$\frac{Y(z)}{X(z)} = \frac{-C_s}{(C_s + C_a)} \cdot \frac{1}{(1 + z^{-4})} \quad (3.46)$$

The actual circuit for this design is implemented differentially as shown in Figure 3.28. The overall working and transfer function remain the same.

As mentioned earlier, the buffer-based switched-capacitor circuit cannot still provide a perfect lossless filter owing to the settling errors of the buffer. The settling error at the sampling capacitor is another major source of error. The accuracy to which these nodes settle (n_{acc}) should be better than that of the overall system so as not to degrade the system SNR. Lower capacitor values in the circuit renders it faster. But, smaller capacitors contribute in terms of thermal noise. It is thus a trade-off between noise and speed. The noise specifications define the minimum capacitor value.

$$\frac{kT}{C_s} + \frac{kT}{C_a} \ll E_{q,tot} \quad (3.47)$$

Once, the capacitors are fixed, the buffer specifications can be derived from settling

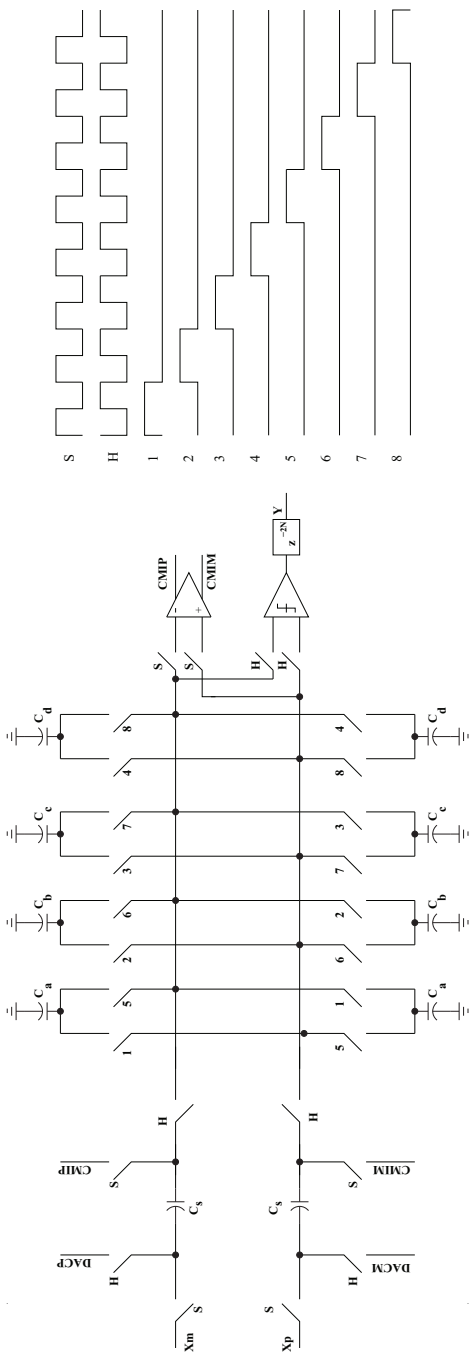


Figure 3.28: Differential implementation of a passive 2-Tone $\Sigma\Delta$ converter

constraints.

$$\begin{aligned}
 t_{total} &= \frac{t_{clk}}{2} = t_{slew} + t_{sett} \\
 &= \frac{C_s * V_{swing}}{I_{slew}} + \frac{\ln(2^{n_{acc}})}{\omega_{UGB}}
 \end{aligned} \tag{3.48}$$

$$\omega_{UGB} = \frac{2\pi f_t C_{gs}}{C_s} \tag{3.49}$$

Knowing C_s from noise and matching constraints, and C_{gs} from the slew constraints, the above equation can be used to determine the limit to which a process can be pushed. To obtain further reduction in power-consumption, techniques such as using clocked comparators and dynamic amplifiers [38] for the buffers can be employed. Though, this is only a 2-tone $\Sigma\Delta$ converter, it can be converted into a generic N-tone $\Sigma\Delta$ converter by adding as many storage capacitors as the transfer function merits. As a general rule of the thumb, an N-tone $\Sigma\Delta$ converter needs 2N storage elements at the least [1].

3.5.2 Capacitor Mismatch Insensitive Design

Figure 3.29(left) shows an active switched-capacitor 2-Tone $\Sigma\Delta$ converter [31]. C_s is the sampling capacitor across which the input is sampled. $C_{a,b..d}$ are the storage capacitors. The outputs are stored consecutively on C_a, C_b, C_c and then C_d . After cycling through all the storage capacitors once, the value of $y[n-4]$ stored on the capacitor is added to the output at the n^{th} instant. The equations that govern this switched-capacitor filter are given by

$$C_s \cdot x[n] + C_a y[n] = -C_a \cdot y[n - 4] \tag{3.50}$$

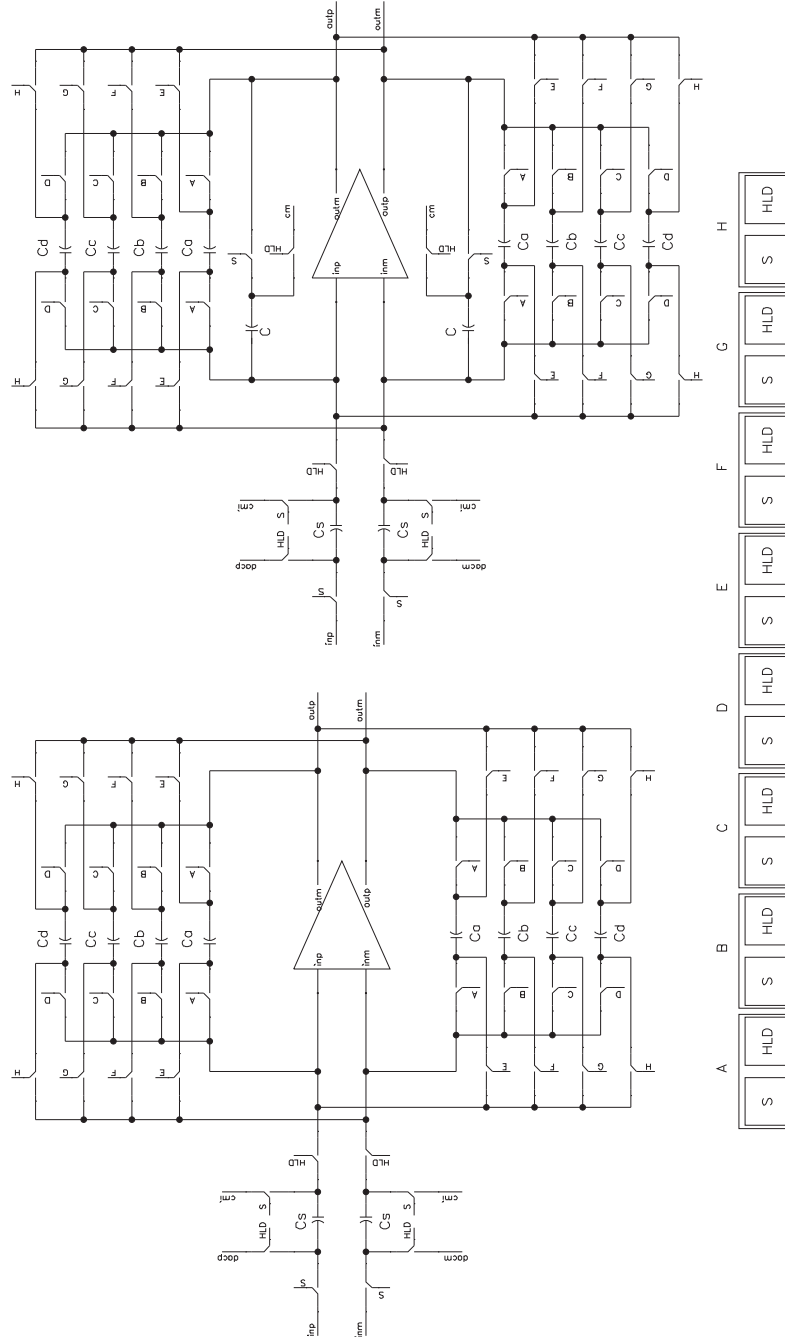


Figure 3.29: Differential implementation of mismatch-tolerant 2-Tone $\Sigma\Delta$ converter

$$\frac{Y(z)}{X(z)} = \frac{-C_s}{C_a} \cdot \frac{1}{(1 + z^{-4})} \quad (3.51)$$

However, owing to the slewing, settling and DC gain errors in the amplifier, the resulting resonator is lossy in nature. Accounting for these error, we see that α and β in the transfer function of the resonator (3.42) can be written as

$$\alpha = 1 - \frac{C_s}{C_a(1 + A)}, \beta = -\frac{C_s}{C_a}(1 - 1/A) \quad (3.52)$$

where $A = A_{dc} \cdot \exp(-\omega t)$, A_{dc} is the DC gain of the amplifier and ω is its UGB. It is possible to ensure that SNR remains well within the required specification by ensuring sufficiently high values for A_{dc} and ω by design.

For the derivation of Eqn(3.51), it is assumed that $C_a = C_b = C_c = C_d$. Capacitor mismatch can cause this assumption to be invalid, in which case, the transfer function varies with time with a period of N/f_s . This will result in harmonics and to avoid this, we can employ an architecture shown in Figure 3.29(right) that is insensitive to mismatch by design [39]. Here, in the 'S' phase, the charge stored on $C_{a..d}$ is transferred on to C along with the input charge from C_s . And, the 'HLD' phase, the charge is transferred back on to $C_{a..d}$ for use in the next $2N^{th}$ cycle. The gain is now $-C_s/C$ and thus, independent of mismatches in $C_{a..d}$ as long as the gain of the amplifier is high. To get better performance, one can use the gain-squaring technique which effectively squares the gain of the opamp [40].

3.6 Measurement Setup

Shown in Figure 3.30 is the test setup for the N-Tone ADC. The chip was mounted on a 2-layer FR4 PCB. The single-ended clock was fed in from an Agilent E2244. The different phases of the clock are derived on-chip from this master-clock. Also provided on-board are the 1V supplies, $REFP = 0.75V$, $REFP = 0.25V$, and a current bias from an external resistor(R_{EXT}). The inputs need to be differential with a common-mode of about 0.6V. A low-voltage differential amplifier is used for the single-ended to differential conversion of the single-ended input to feed into the chip. To calculate the SNR, the output is sampled and stored on a LeCroy 9350AL. With 500MHz BW and 1MB RAM, we get sufficient samples. To view the spectrum with an Agilent Spectrum Analyzer 8560(30 Hz to 2.9 GHz).

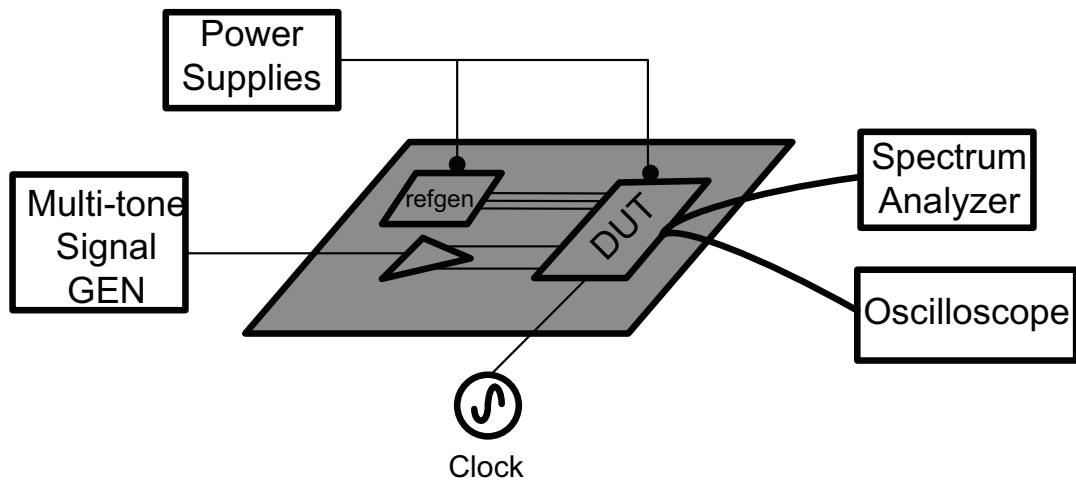


Figure 3.30: Test Setup for the N-Tone ADC

3.7 Conclusions

Various architectures of the N-tone $\Sigma\Delta$ converter and their performance are presented. It is to be noted that the transformation $z^{-1} \rightarrow -z^{-2N}$ can be used to go from a low-pass $\Sigma\Delta$ to its N-tone counterpart. This is in agreement with the well-known fact that $z^{-1} \rightarrow -z^{-2}$ transforms a low-pass $\Sigma\Delta$ into a bandpass $\Sigma\Delta$. System level simulations in MATLAB verify the working of the N-tone $\Sigma\Delta$ converter. Though the SNR reduces by a factor of $20 \log(N)$, it is still a viable candidate for the UWB-OFDM receiver as the SNR required in such systems is small (only 8dB in one implementation). This can be attributed to the fact that we now occupy $N \cdot f_b$ of entire available spectrum as against just f_b in the low-pass converter. Also, non-idealities like thermal noise, amplifier non-idealities and capacitor mismatch, were modeled at a system-level in MATLAB to study their effects. The non-idealities were found to degrade SNR and introduce undesired tones in the spectral response. A low-power implementation of a 2-Tone $\Sigma\Delta$ converter is presented and design issues are discussed. This 2-Tone $\Sigma\Delta$ converter can be very easily extended to a generic N-Tone configuration. However, like every other first-order $\Sigma\Delta$ converter, it is extremely tonal which calls for the need of a higher order N-Tone $\Sigma\Delta$ converter. Also, an architecture that is inherently insensitive to capacitor mismatch has been adapted to the N-tone $\Sigma\Delta$ converter.

Chapter 4

Multi-lane PRBS Generator

A low-power three-lane 2^{31} pseudo-random binary sequence (PRBS) generator was designed by multiplexing four appropriately delayed parallel sub-sequences running at one-fourth the data rate. The prototype PRBS generator fabricated in a $0.18\mu\text{m}$ CMOS process operates at 5Gbps. The total measured power consumption is 218mA off a 1.8V supply which translates to $\approx 131\text{mW}$ per lane. The calculated figure of merit for this all-CMOS design is 0.84pJ/bit which is better than other published designs.

4.1 Motivation

High-speed serial links continue to evolve and with technologies like PCI Express and Hypertransport, data-rates have moved into the multi-Gbps range. As more and more transceivers are built in the multi-Gbps range, it seems not only more economical but also practical to have on-chip data generators and BER calculators, to avoid having to deal with the effects of the package parasitics. Normally, in a single transceiver system, having a PRBS length of $2^{31} - 1$ ensures that the system can handle random data by stressing it with every permutation of a 31-bit sequence. In a multi-transceiver system, besides ensuring that each transceiver operates correctly, it is necessary to ascertain that data streams to neighboring channels are minimally correlated. To study the effect of cross-talk between multiple channels in a transceiver, one requires multiple streams of data that are non-correlated and a clock that is synchronous with the data for test [41, 42].

Most of the previously reported state-of-the-art high-speed PRBS generators are developed in technologies like HBT, BiCMOS and SiGe [43] [44] [45]. But, CMOS still presents itself as the technology of choice for the ease of integration with digital processors and the low-cost. Hence, the need for on-chip CMOS PRBS generators.

In this chapter, we describe a PRBS generator that was used to drive a transmitter with cross-talk cancelation circuits. The design while being a low-power solution, also validates optimizations made to two traditional high-speed circuits - a cross-coupled CMOS latch and a CML MUX with active inductor load for bandwidth extension.

4.2 Pseudo-Random Data Generator Architecture

The most prevalent way to generate high speed sequences of length ‘N’ is by multiplexing ‘q’ lower data-rate sequences ‘f’ [46]. The resulting sequence will be at a data-rate of ‘ $f \cdot q$ ’. The data-rate one can achieve is then limited by the speed of the multiplexer. Also, the level of multiplexing determines the power. As it increases, the core does consume low power but the multiplexer and the delay elements start consuming a lot of power.

The lower-data rate sequences can be generated in either a series or parallel fashion. In the series architecture, ‘q’ lower data-rate sequences are phase shifted by $(N - 1)/q$ bits and then multiplexed. As the number of sequences to be multiplexed increases, so does the number of XOR gates required and hence the power. In parallel architecture, phase-shifted sequences are obtained by using a transition matrix of the characteristic polynomial [5]. Though the series-parallel architecture uses more XOR gates, it makes for a robust design as it avoids the problem of tuning the delay elements over process and temperature. As parallelism, N, increases, the LFSR consumes less power due to its lower operating speeds; but, the overall design might consume more power due to the overhead of timing/XOR elements and multiplexers (MUXes). Therefore, a careful selection of the amount of parallelism is required for a power-optimal design. Operating at data rates close to the f_T of a process results in a high-power clock-tree and a power overhead due to second-order effects [citeprbskatti]. In order to operate a large part of the design at lower speeds so as to use low-power CMOS circuits, we choose $N =$

4. Only the high-speed MUXes are implemented as power-hungry CML circuits. This careful system-partitioning into CMOS and CML along with using only one LFSR core for multiple PRBS streams results in lower power as compared to published designs.

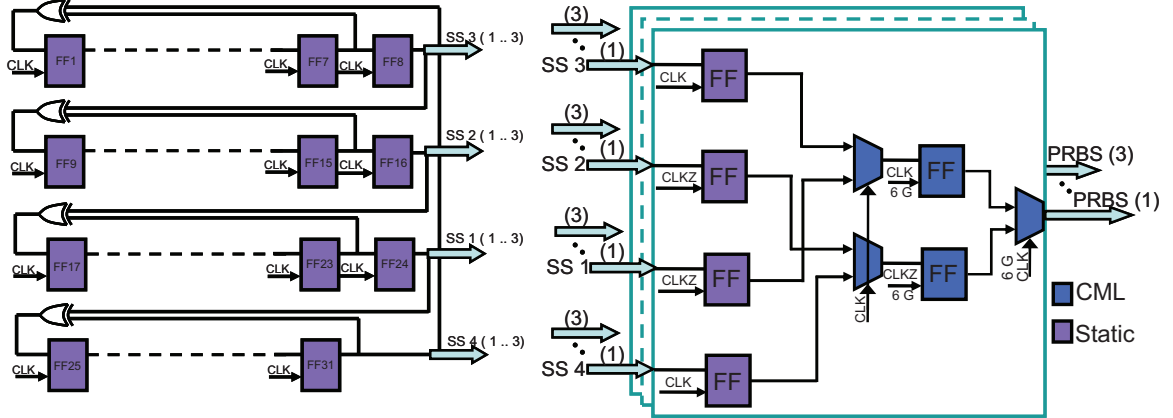


Figure 4.1: Block diagram of the series-parallel LFSR and PRBS

In this design, the linear feedback shift-register (LFSR) is configured in a series-parallel fashion to generate four parallel subsequences at $3Gbps$ which are then multiplexed up to $12Gbps$ (Figure 4.1). Previously reported series-parallel architecture employs CML circuits and operates at higher speeds while our design uses a mix of CMOS and CML circuits. To describe the implementation in detail, the PRBS generator takes as its inputs - two CML clocks running at $3GHz$ and $6GHz$. While the CML clocks are used to drive the high speed CML MUXes, the $3GHz$ clock is also translated to CMOS levels, so as to drive the CMOS latches. The CML-to-CMOS converter used is briefly described in the section 4.3. The LFSR implements the primitive poly-nominal to give the maximal length binary sequence for a 31-bit shift-register.

$$P = 1 \oplus x^{28} \oplus x^{31} \tag{4.1}$$

The series-parallel quarter-rate LFSR is realized by implementing the T^4 transition matrix of the polynomial $1 + x^{28} + x^{31}$. As always, to prevent a stuck-at-zero condition in which the PRBS will fail to start-up, we use a system RESET pulse that resets the entire shift-register. The four shifted sequences are then delayed appropriately so as to be setup ideally for the CML MUX. Though the $3GHz$ and $6GHz$ clocks are aligned in simulations, a variable delay is included in case we need to align the clocks to account for process mismatch.

4.3 Circuit Design and Implementation

The major blocks in the PRBS Generator are the high-speed latch, high-speed MUX and the CML-to-CMOS converter. This section presents the design of these individual blocks [47].

High-Speed CMOS Latch

As shown in Figure 4.2, the CMOS latch consists of primarily switches in the track-phase which pre-charge the storage nodes (Q, QZ). In the hold-phase, the latch is just the traditional back-to-back inverters forming the regenerative structure with positive-feedback that holds the sampled value. Rather than use the regenerative latch to do most of the work, which will directly mean a longer latch-time indirectly a longer sample-time

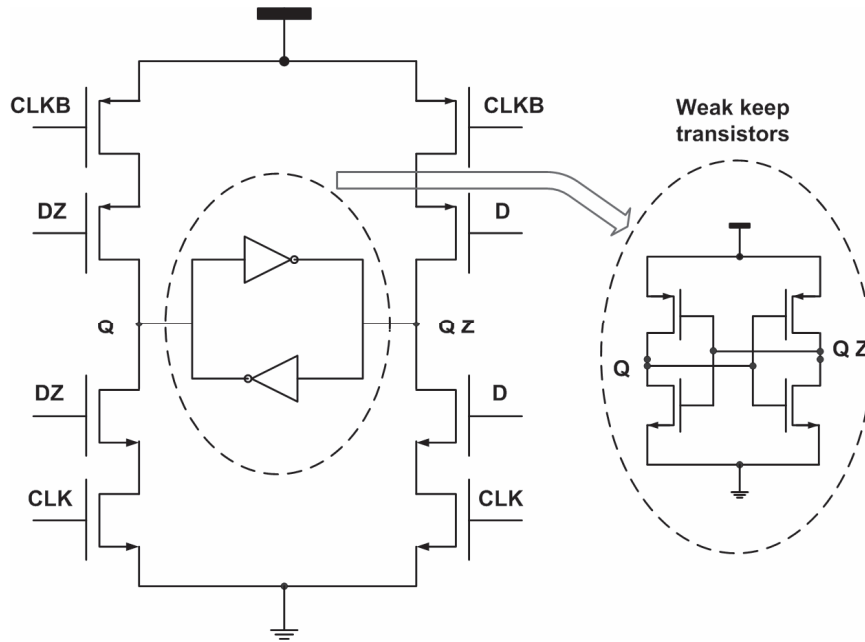


Figure 4.2: Circuit diagram of CMOS latch

because of the loading at the storage nodes (Q, QZ), we use it like a dynamic latch. The switches pre-charge both the storage nodes completely to either the supply or ground voltage levels. And the regenerative latch just act as weak keep-transistors. In other words, using the well-known result that the regeneration time of such a latch is given by

$$T_{latch} = \frac{K \cdot L^2}{\mu \cdot V_{eff}} \cdot \log\left(\frac{V_{logic}}{V_0}\right) \quad (4.2)$$

It is obvious that the latch time is inversely proportional to the initial voltage across the latch as it enters the regenerative phase. To take advantage of this, in the track phase, we pre-charge both Q and QZ. This is done by having series NMOS and PMOS switches which are gated by the clock and data. As the outputs are pre-charged to the

final values, the regenerative latch can be as small as possible which in turn means that the parasitic capacitance that the pre-charge switches have to charge is small. This results in a smaller load on the track-phase switches, enabling the latch to run at high-speeds. Of course, this means that the output nodes are sensitive and one has to pay attention to layout to ensure minimal coupling from any noisy nodes to the storage nodes. It is important to note that, in this process, the highest speed one can achieve from this architecture is now limited by the R_{on} of the PMOS switches. Since this was a custom-design, the latches were designed to account for a maximum fan-out of two - the succeeding latch in the shift register and wire-parasitics.

$$F_{max} = \frac{1}{4.4 \cdot R_{on} \cdot C_L} \quad (4.3)$$

$$F_{max} = \frac{f_T}{4.4 \cdot fanout} \quad (4.4)$$

It can be noted that the maximum achievable frequency is now a factor of the f_T of the device. The PMOS being the device with the lowest f_T is now what dictates the highest attainable frequency. In this process, with a PMOS f_T of approximately $25GHz$, this would be limited to about $3GHz$. Also, the position of the clock and data switches were interchanged in the first latch fed by the XOR gates, to account for the delay in the XOR gate. This ensured that the latest arriving signal was always closer to the output.

High-Speed CML Multiplexer

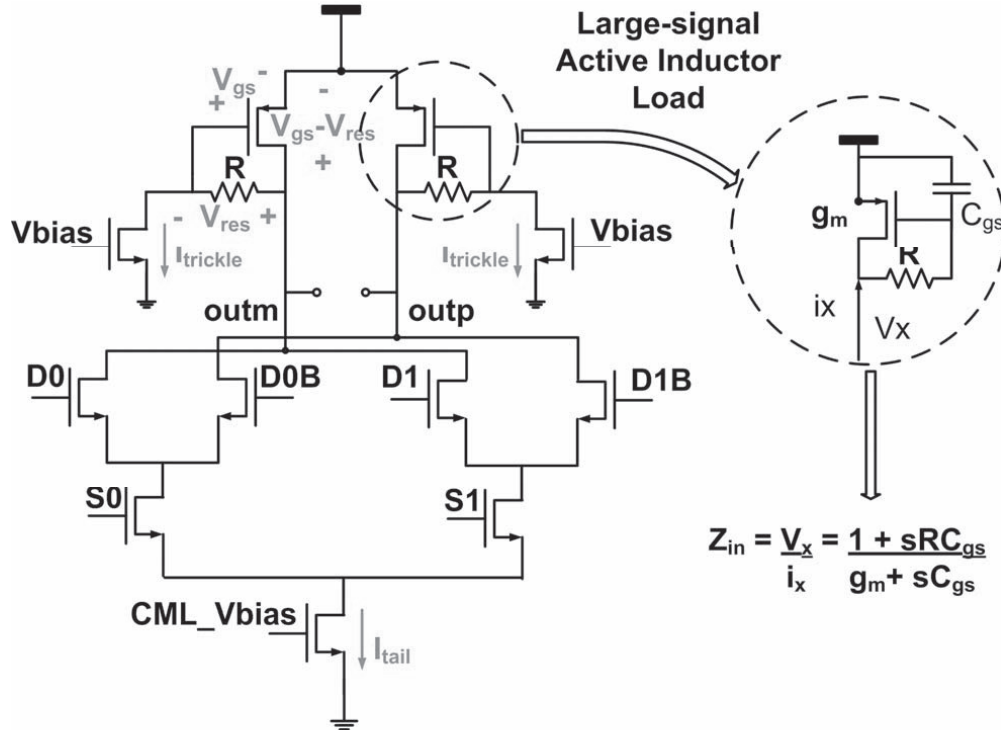


Figure 4.3: Circuit diagram of CML MUX

Since the PMOS has low f_T , to realize a high-speed MUX with a full peak-peak swing of $0.5V$ at $12Gbps$, we choose a CML architecture which employs the high-speed NMOS and passive resistors. Further, the bandwidth of CML logic is extended to $6GHz$ from approximately $3GHz$. There are several existing techniques for bandwidth-extension such as the usage of peaking inductors or Cherry-Hooper amplifier [48]. Although both techniques extend the bandwidth of the design, inductive peaking requires too much area for its inductors and the Cherry-Hooper amplifier consumes too much power. Active inductor load, which consists of a PMOS transistor with a resistor connecting

the gate and the drain, has also been used to extend bandwidth for small signal swings by introducing an inductive term as shown in the small signal analysis refeqn:ind [48]. However, it is obvious that as the current through the load changes during large-voltage swings, the g_m of the PMOS varies significantly, causing the small-signal impedance to also fluctuate drastically. Thus, using active inductor loads in CML logic circuits will distort the large signal behavior due to the continually changing load impedance.

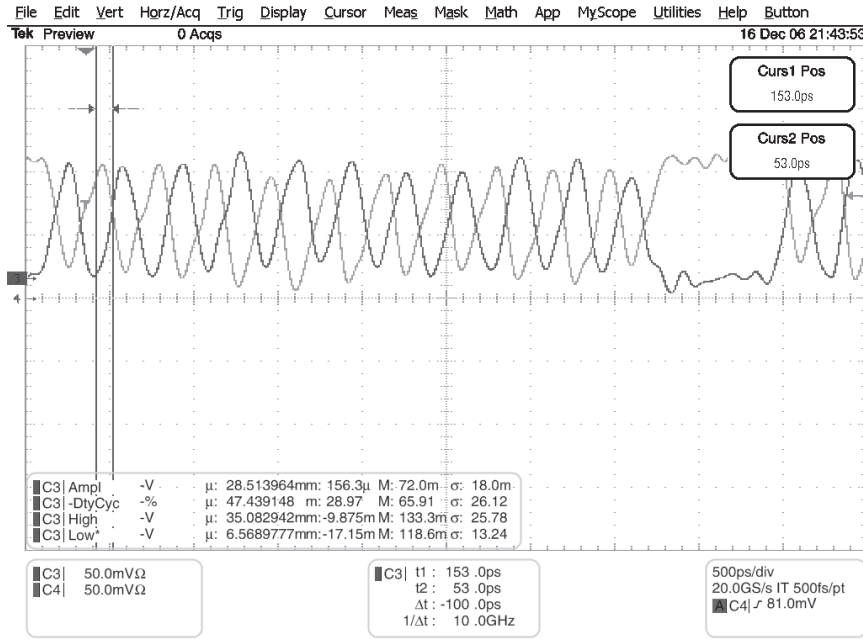


Figure 4.4: Time domain plots of the 12Gbps PRBS

$$Z_{in}(s) = \frac{V_x}{i_x} = \frac{1 + sRC_{gs}}{g_m + sC_{gs}} \quad (4.5)$$

Figure 4.3 shows a modified active inductive load which has an additional current source attached to the gate of the PMOS. The current source improves the bandwidth of the circuit through two mechanisms. First, headroom is increased by producing a voltage

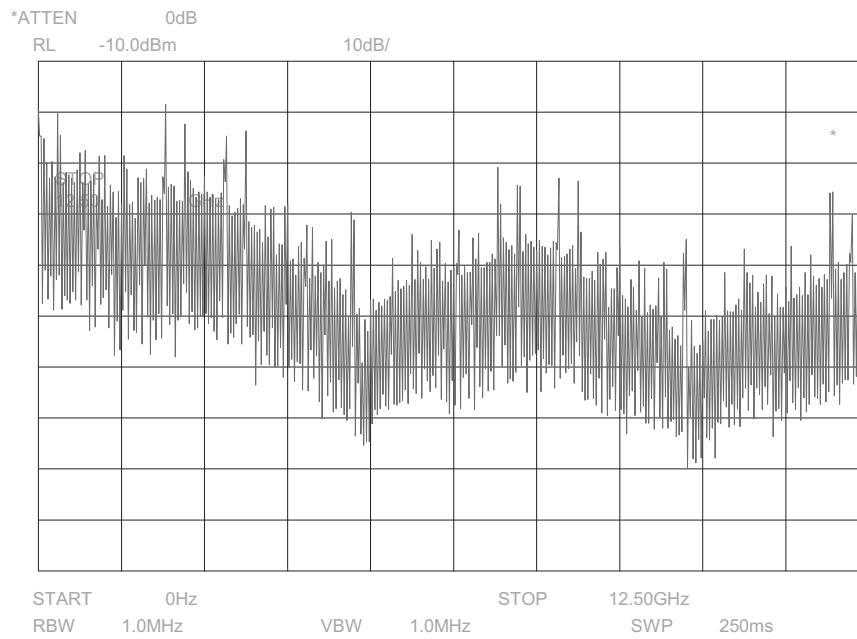


Figure 4.5: Frequency domain plots of the 12Gbps PRBS

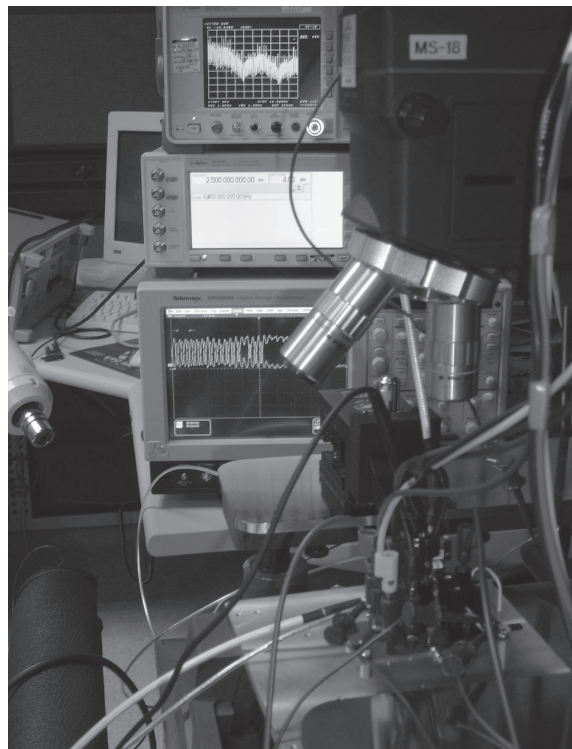


Figure 4.6: Measurement setup for the 12Gbps PRBS

drop across the resistor so that $V_{ds} < V_{gs}$. Second, it provides current to the PMOS during the off state so that gm is only 3 to 4 times lower compared to g_m during the on state. This means that the inductive term is still introduced and the effective impedance remains relatively steady during large swings reducing the large-signal distortion.

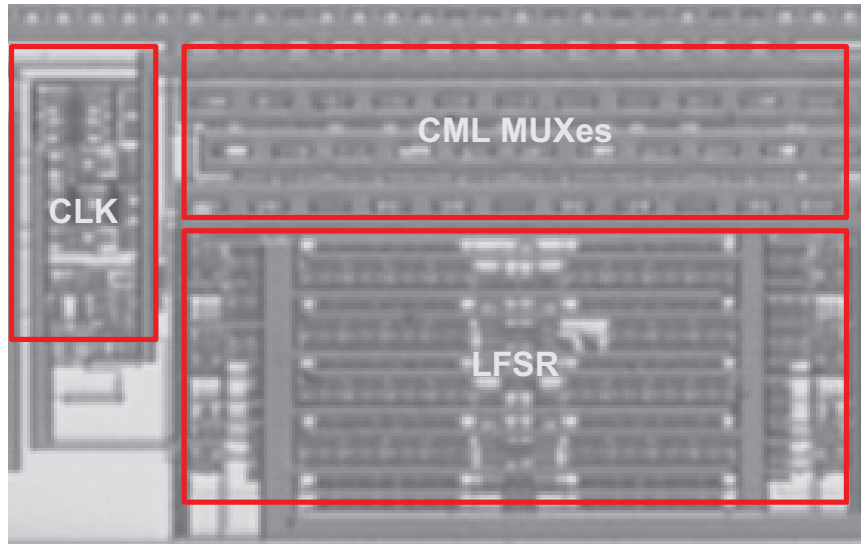


Figure 4.7: Die photo of the PRBS generator

The delay of the CMOS clock-path the sum delay of the CML-to-CMOS converter and the CMOS clock-tree has to match to the delay of the CML clock-tree to ensure functionality. Though the timing of the signals was verified by extensive parasitic RC simulations in SpectreRF, a variable delay was included in the CML clock path for post-fabrication tunability. The variable delay is implemented using positive feedback. A negative resistance cell is placed in parallel with the resistive load of a CML buffer and the delay is controlled without altering the output swing by varying the current through the buffer and the negative-gm cell differentially

4.4 Measurements

The design was fabricated in the $0.18\mu\text{m}$ TSMC process and occupies $2.7\text{mm} \times 1.9\text{mm}$ as shown in Figure 4.7. Operating at 5Gbps , the chip consumes 73mA per lane off a 1.8V supply. The PRBS data is buffered out to the RF probe pads using a tapered CML buffer with 50F load. By using AC-coupled GSGSG probes, the transient waveform measured with a Tektronix TDS 6804B (Figure 4.6) shows a rise time of $\approx 100\text{ps}$ as in Figure 4.4. The frequency-domain plot of the PRBS data, measured with an Agilent 8563, shows a peak at 2.5GHz which is exactly half the data rate as in Figure 4.5 [51].

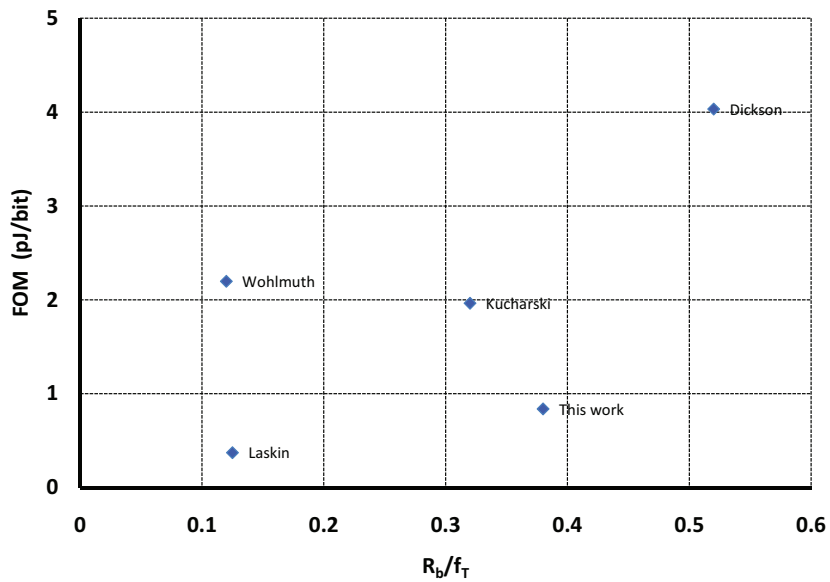


Figure 4.8: FOM comparison

4.5 Conclusions

To ensure a fair comparison to other existing designs, we use the figure-of-merit (FOM) as defined in [45]

$$FOM = \frac{power}{\log_2(length) \cdot speed} \quad (4.6)$$

Using this definition, the FOM of some of the prior state-of-the-art designs have been calculated and tabulated in Table 4.1. The FOM for our prototype is calculated to be 0.84 pJ/bit. This is lower than previously published designs as seen in Figure 4.8.

Table 4.1: FOM calculation

	Process	Power (mW)	Length (bits)	Speed (Gbps)	FOM (pJ/bit)
Laskin et.al [44]	SiGe	60	$2^7 - 1$	23	0.37
Kucharski et.al [43]	SiGe	550	$2^7 - 1$	40	1.96
Wohlmuth et.al [49]	120nm CMOS	205	$2^7 - 1$	13	2.25
Dickson et.al [50]	SiGe BiCMOS	9800	$2^{31} - 1$	72	4.39
This work	130nm CMOS	131	$2^{31} - 1$	5	0.83

Chapter 5

Future Work and Conclusions

Clocking is probably one of the most important aspects of design. Both digital and analog designs face this design challenge. Digital designs, because they are inherently synchronous to a system clock and analog designs because of their transducer properties as they convert real-time analog inputs to discrete digital signals. In the ADCs discussed in Chapter 2 and 3, the design and distribution of the non-overlapped sample and hold phases is as important as the analog aspects of the design. In the high speed PRBS design discussed in Chapter 4, the partitioning of the circuits and hence the clocking into CMOS and CML distributions is an important facet of the power optimization of the overall design. The problem of clocking only gets bigger and more complicated as digital processors move towards the "Many Integrated Core Architecture" (MICA) to harness parallelism in an effort to increase throughput(Figure 5.1) [52]. There is not just the problem of delivering the system/processor clock to all the cores, but also the issue of distributing the reference clocks to all the PLLs and DLLs controlling the IO buses.

Shown in Figure 5.2 is Intel's first general-purpose MICA-based server. Code-named Knight's Ferry it has 32 cores running at $1.2GHz$ and capable of processing 128 threads simultaneously at 4 threads/core. It also has $1-2GHz$ GDDR5 as the memory interface and a host of other I/O interfaces [52].

And true to the magnitude of the problem, lots of research has been geared towards clock distribution [53], [54], [55], [56]. In summary, the CML and CMOS clock

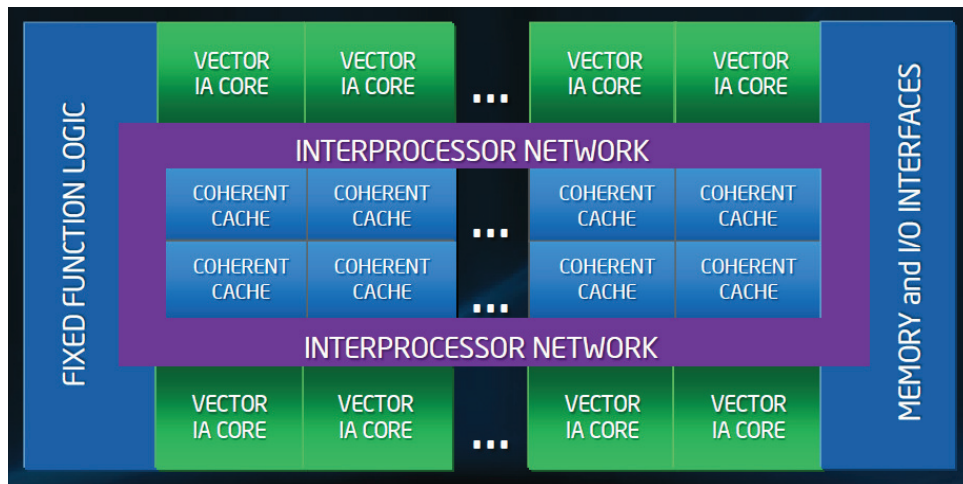


Figure 5.1: Many Integrated Core Architecture

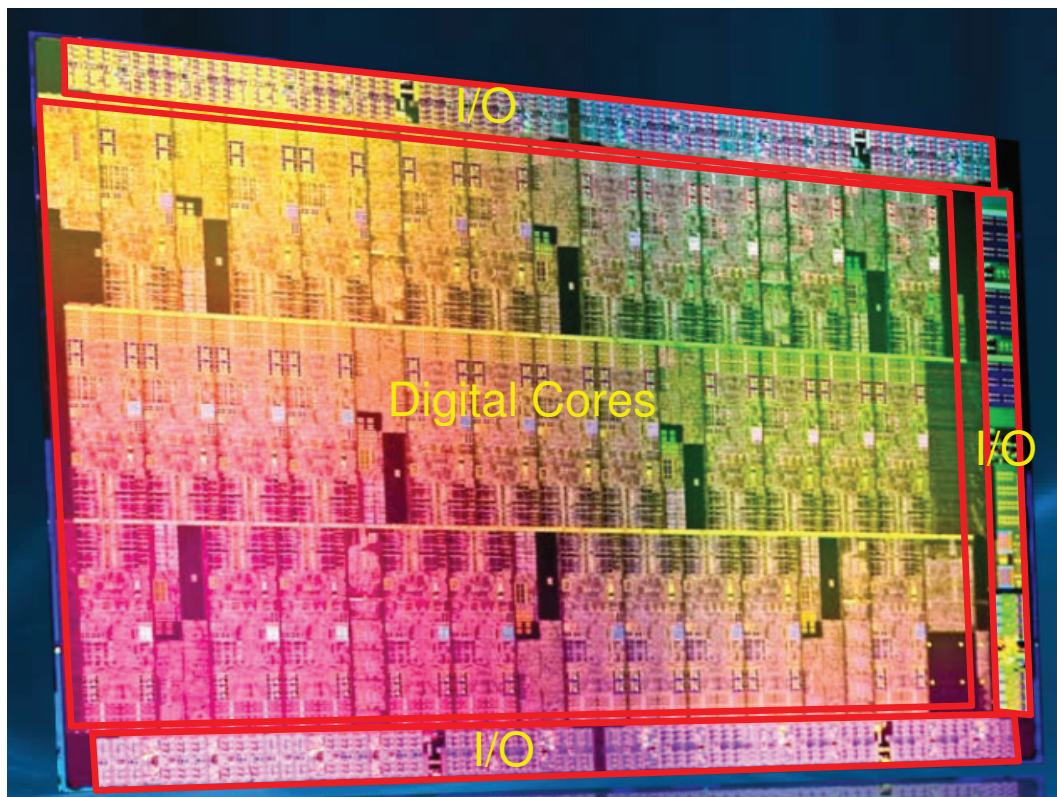


Figure 5.2: Knights Ferry

distribution of Chapter 4 are the basic forms of clock distribution with CMOS distribution turning out to be better in terms of jitter and power if the clock-frequencies are not close to the f_T of the process. The repeater-less clock distribution described in [53] is by far the best in jitter-performance, the power dictated by the driver of the T-Line (Figure 5.3). This can be taken a step further at the cost of area by employing inductive-boosting [54]. But for the frequencies of reference clock to the PLL i.e. a few hundreds of MHz, a T-Line distribution is the best in terms of jitter, power and floorplan driven constraints.

The impedance of the T-Line does not need be 50Ω , since the clock needs to be distributed only on-die and never leaves the chip. The higher Z_o allows for lower power consumption in the driver. Also to be noted is that the T-Line is terminated only on the driver side, this allows for full-swing at the far-end and reduces reflections from the driver side.

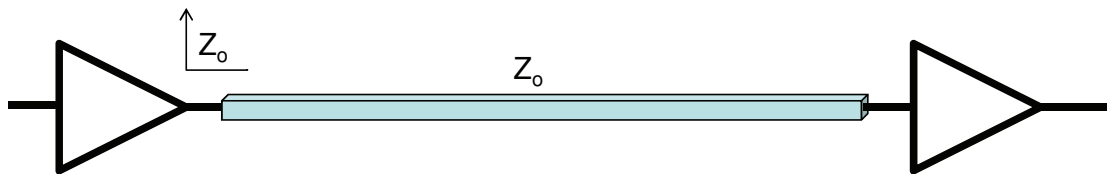


Figure 5.3: Repeaterless Clock Distribution

The floorplan driven constraints are not something you encounter in a pure analog design. But, when the analog circuits nestle in a digital environment, for example - the

”many” digital processors - this becomes utmost important. To realize the least lossy transmission line, one is bound to pick the top-level metal available in the process [57]. Unfortunately, this is also the preferred layer for power-delivery. Using this top-level metal for the T-Line will compromise the robustness of the power delivery network. And when the minimum width of these layers are dictated by the process DRC rules, using it for power delivery of the repeater chain driving the T-Lines will cost a significant amount of real-estate.

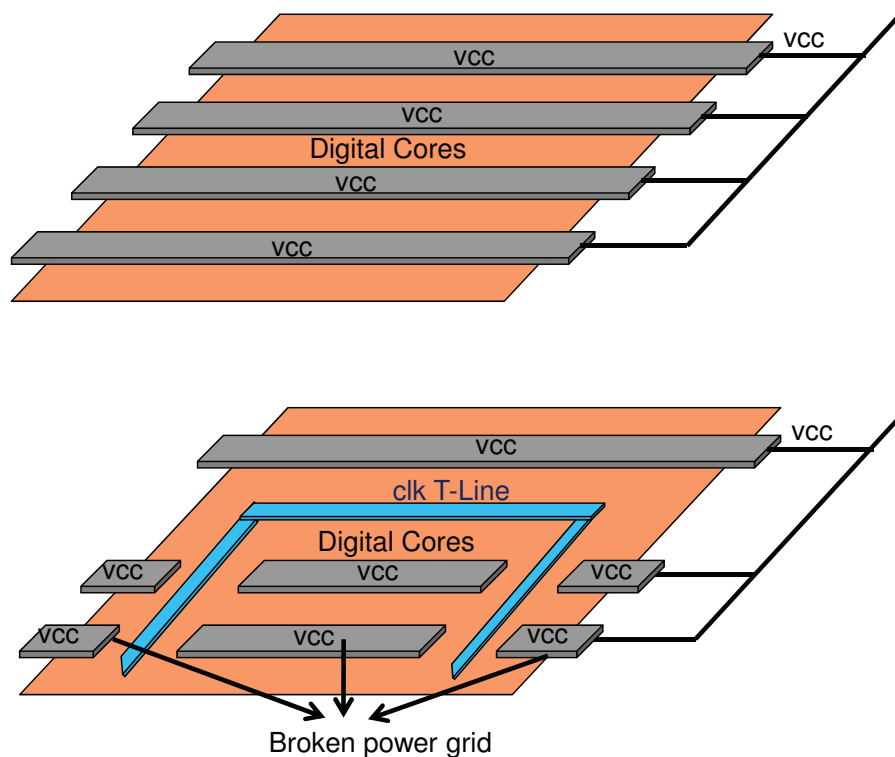


Figure 5.4: Floorplan constraints

In flip-chip bonding on a build-up substrate - which has been the preferable solution

for high performance system - a smaller micro-via technology is sought after to achieve higher density. The diameter of the micro-vias in the first build up substrate was $127\mu\text{m}$ [58] [59]. And recently a $25\mu\text{m}$ micro-via was reported [60]. Such micro-vias can be used to deliver power to the clock buffers thus mitigating the adverse effects of using multiple tracks of top-level metal. This also brings in another advantage of being able to use a supply different from the core-power supply to drive the clock distribution. This external power supply can now be filtered on the package for a better supply noise profile and hence better jitter. Also, this power supply can have a much higher DC level like the I/O as compared to the digital core for a low-jitter design.

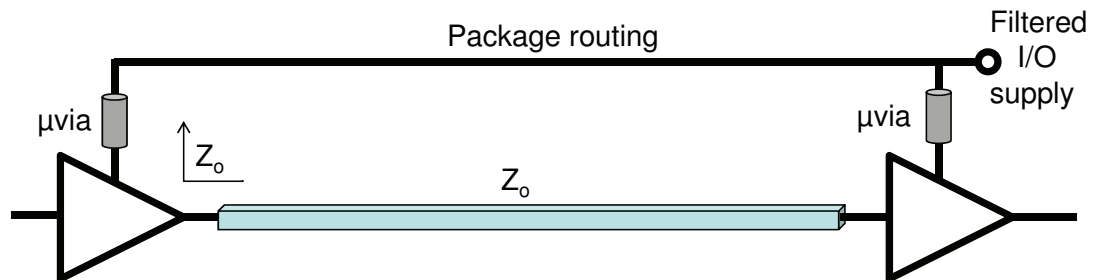


Figure 5.5: Repeaterless Clock Distribution with filtered supply

5.1 Conclusions

In conclusion, it is to be noted that as CMOS processes become more and more digital-friendly and in fact, analog agnostic, the demarkation between analog and digital domains is becoming more porous. Designs can no longer be purely analog. They have to be either digital-process-friendly architectures or digitally-assisted. The designs have

to look at the system as a whole since often, the optimal design can only be realized by trading off analog and digital design spaces, or on-die and off-die designs. This thesis presented a study of the process trends in Chapter 1. Chapter 2 and 3 both present variations of the $\Sigma - \Delta$ architecture for an ADC which lends itself favorably to such digital processes while trading off resolution in time-domain for resolution in voltage domain. Chapter 2 presents a multi-rate $\Sigma - \Delta$ ADC which is a hybrid between a continuous-time and discrete-time $\Sigma - \Delta$ ADC that reduces the constraints on the anti-aliasing filter preceding the ADC. The Multi-tone $\Sigma - \Delta$ ADC presented in Chapter 3 is designed to specifically complement the multi-tone nature of the UWB signal. Chapter 4 uses amortization and optimal partitioning into CMOS and CML domains for a power-efficient PRBS generator. In the final chapter 5, a power-efficient clock distribution is presented which takes advantage of advances in the packaging technology to deliver a low-jitter clocking solution in a digital environment.

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