

**Design and Analysis of CMOS LC Voltage Controlled  
Oscillator in 32nm SOI Process**

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**Chris H. Kim**

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# Dedication

This thesis is dedicated to my family.

## Abstract

This thesis deals with the design and comparative analysis of different architectures of on-chip LC voltage controlled oscillators. The design is implemented using IBM 32nm design process and the kit inductors and varactors are used to make the resonator. Different VCO architectures have been studied in terms of their phase noise, tuning range, voltage swing and the area. The aim of this thesis is to provide proper analysis and design of a low noise, robust voltage controlled oscillator in the 32nm SOI design process.

A maximum tuning range of approximately 800 MHz is achieved with the best case phase noise performance of -116.16 dBc/Hz at 1 MHz offset by using the best architecture. For this design the power consumption is 1.63mW at 0.9V supply voltage and normal operating condition of 25°C.

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# Chapter 1

## Introduction

A voltage controlled oscillator is the key element of the frequency synthesizer and it has a huge impact on its overall performance. VCOs are the critical component of RF transceivers and are used to perform signal processing tasks such as frequency selection and signal generation. In digital circuits, oscillators are used to synchronize the operations using a reference clock. VCOs are generally used in the feedback loop of phase locked loops (PLLs) to provide an accurate reference clock. A simple PLL implementation is shown in figure 1.1. The circuit evolutions over time in terms of accuracy and speed necessitate the use of VCOs with center frequency in the Gigahertz range.

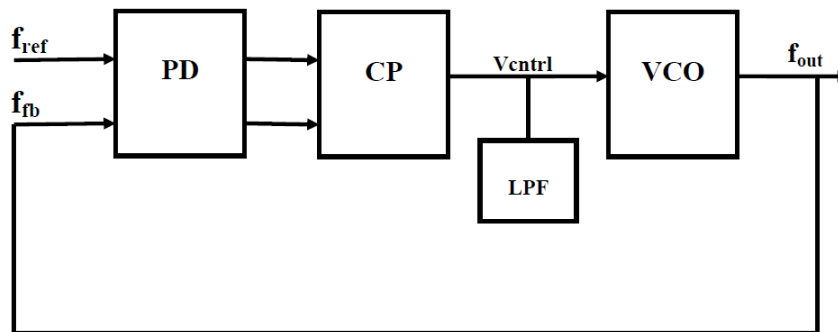


Figure 1.1: PLL Block Diagram

The design of first silicon monolithic VCO dates back to 1992 [1] and after that there

has been a rapid growth in terms of on chip VCOs with the shrinking of technology. The development of VCOs is shown in Figure 1.2 [2].

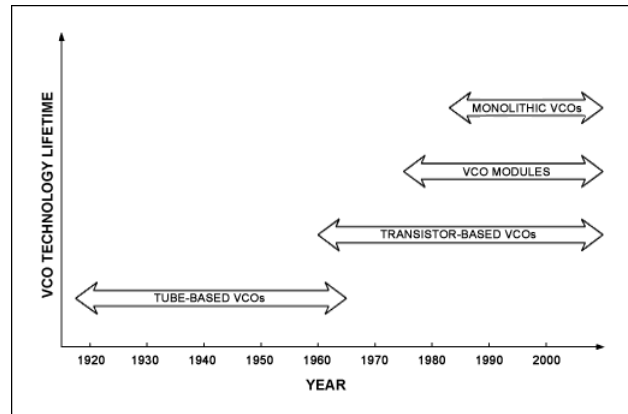


Figure 1.2: Evolution of VCOs [2]

In the CMOS based VCO design there are two types [3] which are used, which are:

- Ring based VCO
- LC based VCO

In terms of phase noise performance LC VCOs have been proven to be better than ring based VCOs, but it is inferior in terms of tuning range, layout area and sometimes power consumption [4]. With the recent increase in the clock speed and the advancement of multi-GHz circuits, it has become important to have an accurate jitter performance which is getting harder to satisfy using ring VCOs [5], thus making LC VCO an obvious choice. Figure 1.3 [5] explains the comparison of ring based VCO and LC based VCO in terms of jitter, power and area for 90nm design process.

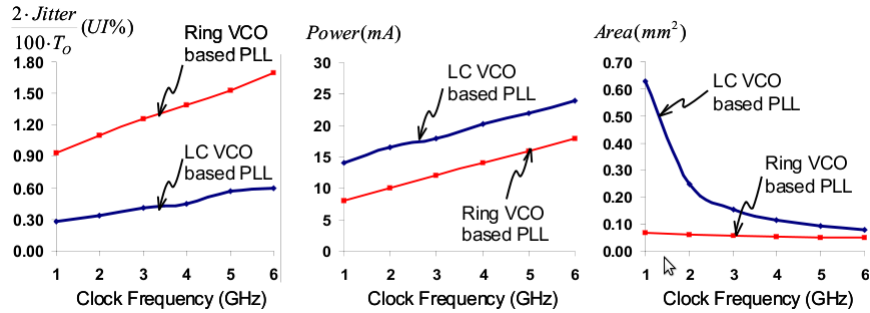


Figure 1.3: Jitter, power and area comparison of ring VCO and LC VCO [5]

As the clock speed reaches 4 GHz and above the area overhead of LCO VCO is insignificant whereas the jitter performance is enhanced multiple times. In this work, different architectures of VCOs on IBM 32nm SOI process are simulated and their performances are compared based on the measurement results. The VCOs are compared in terms of phase noise, tuning range, power and size.

## Chapter 2

# LC VCO Basics

A voltage controlled oscillator, in its basic form, is a circuit which has a  $V_{tune}$  as an input and an oscillating output  $V(t)$ . It is connected to power supply and ground rail as shown in figure 2.1.

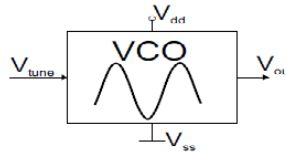


Figure 2.1: Basic VCO [6]

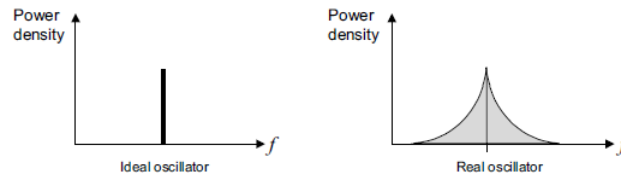


Figure 2.2: Frequency spectrum of ideal and real oscillator [6]

The center frequency of oscillation is a function of the tuning voltage input shown as  $V_{tune}$ . An ideal VCO oscillates at a center frequency commonly termed as  $f_c$ . But in

real situation the output fluctuates from its center frequency and is shown in figure 2.2 [6] which corresponds to jitter in time domain.

Reference	Tech ( $\mu\text{m}$ )	Frequency (GHz)	Phase Noise (dBc/Hz)	Power (mW)	Voltage (V)
Hajimiri [7]	0.25	1.8	-121 @ 600Khz	6	1.5
Vora [8]	0.6	2	-103 @ 100Khz	22	NA
Andreani [9]	0.8	2.4	-118 @ 1Mhz	22.5	2.5
Razavi [10]	0.6	1.8	-100 @ 500Khz	7.59	3.3
Lam [11]	0.35	2.6	-110 @ 5Mhz	13	2.5

Table 2.1: Reported LC CMOS VCOs performances

Frequency tuning refers to the range the center frequency of the oscillator can be changed with the use of tuning voltage. The more this variation, the better is the design in terms of controllability. Phase noise is one of the most important parameter which a designer has to focus while designing the VCO. A comparison of different parameters for VCO from different papers are listed in table 2.1.

## 2.1 Oscillator Models

Every LC oscillator can be treated as a feedback network as shown in figure 2.3.

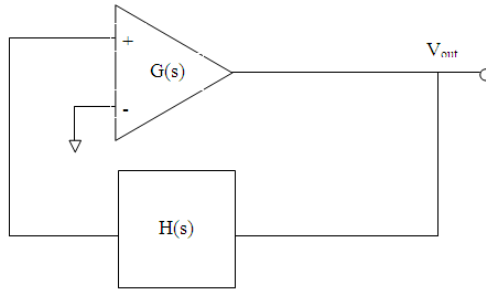


Figure 2.3: Feedback oscillation model

Barkhausen criteria define the conditions for oscillation. The first criterion states that the gain around the feedback loop should be equal to unity. The second states

that the total phase shift around the loop should be  $0^\circ$  or a multiple of  $360^\circ$ . This is an approach which has widely been used to explain the oscillator performance. Another approach is to describe the operation of oscillators in terms of negative resistance. The LC tank provides the positive resistance whereas a transconductance amplifier ( $G_M$ ) provides the negative resistance ( $-1/G_M$ ) which is seen by the LC tank. It was shown in [12] that if the Barkhausen stability criteria are satisfied then the negative resistance exactly cancels out the parallel resistance of the LC tank. Intuitively, the losses in the tank dampen the oscillation and the active devices add energy back to the system to make the oscillations continue. A symbolic representation of  $G_M$  is shown in Figure 2.4a.

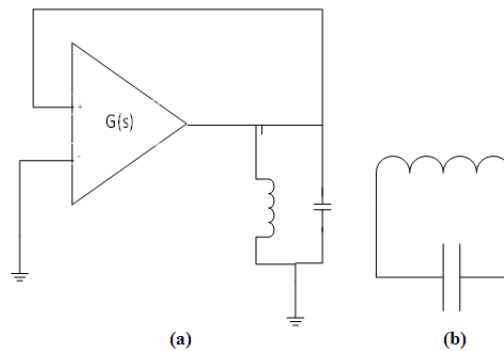


Figure 2.4: (a) Negative transconductance model (b) Parallel LC tank

## 2.2 LC Tank Basics

LC tank is basically a series or a parallel connection of an inductor and a capacitor. A parallel configuration is same as the one shown in figure 2.4(b). It can store energy and oscillates at its resonant frequency. The energy oscillates between the inductor and the capacitor until the internal resistance of the LC tank dampens it and finally it dies out. The frequency of oscillation is determined by the value of inductance and the capacitance used. According to the Kirchhoff's law the voltage across inductor and the capacitor should remain the same. Hence  $V_C = V_L$ , in the same way the current flowing through both the inductor and the capacitor should also be the same and thus

$I_C = I_L$ . As we know

$$\begin{aligned} V_L(t) &= L \frac{\partial i}{\partial t} \\ i_C(t) &= C \frac{\partial V}{\partial t} \end{aligned}$$

Using the above two equations we can get a second order differential equation which is

$$\frac{\partial^2 i}{\partial t^2} + \frac{i(t)}{LC} = 0$$

A parameter  $\omega$  is defined as  $\frac{1}{\sqrt{LC}}$  and thus the equation becomes

$$\frac{\partial^2 i}{\partial t^2} + \omega^2 i(t) = 0$$

The solution for this differential equation is

$$i(t) = Ae^{j\omega t} + Be^{-j\omega t}$$

The solution of the above equation is a sinusoidal alternating current. If we assume  $A = B$  then according to the euler's formula the current will represent a sinusoid with an amplitude of  $2A$  and angular frequency of  $\omega = \sqrt{LC}$ . Thus

$$i(t) = 2A \cos(\omega t)$$

and the central frequency of oscillation is given by

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

### 2.3 LC VCO Topologies

There are several LC VCO topologies present which use the CMOS cross coupled structure to provide the negative resistance. In this work, three different LC VCO architectures have been studied. Performance parameters such as the central frequency, tuning range, phase noise, power and area have been considered. In a broad sense, LC VCO can be organized into NMOS LC VCO, PMOS LC VCO and NMOS PMOS LC VCO. The LC VCOs examined are shown in figure 2.5, figure 2.6 and 2.7. Each of the architectures have different advantages and disadvantages over others in terms of the performance parameters and is explained in this section. A more detailed analysis is done in the result section where the results are shown for this comparison.



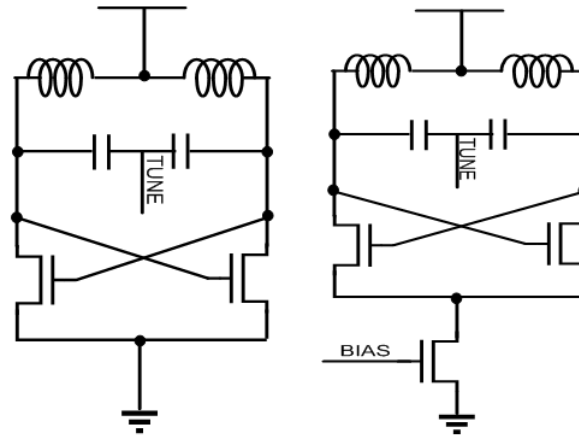


Figure 2.5: (a) NMOS VCO; (b) NMOS VCO with footer

In figure 2.5 LC VCO designed on NMOS transistor is shown. It has two inductors, two capacitors and a cross coupled NMOS switches. The tank is made by inductors and the capacitors. The negative resistance for the device is given by the transconductance of the cross coupled NMOS devices. In the VCO the capacitor is basically a varactor whose capacitance changes with the tuning voltage. The varactors are separated from the power supply by the inductors and from the ground by the cross coupled NMOS pair. The inductors are directly connected to the power supply. This makes the VCO more prone to the disturbances from the supply [13].

In figure 2.5 LC VCO is designed using the similar fully NMOS topology but it also provides a NMOS based tail current source. This tail current source gives the designer to limit the supply current which also decides the total power consumption. This controllability of the supply current gives the designers a method to control the negative resistance of the cross couple NMOS pair which in turn controls the oscillation amplitude. However, in [14] it has been shown that the phase noise performance of the VCO is improved by completely removing the tail current source. So, basically its a trade off between controllability of the design, power consumption and the phase noise performance.

Figure 2.6a shows the LC VCO based on PMOS transistors. The design is totally complimentary to the figure 2.5a. For comparison purposes it is good to analyze this

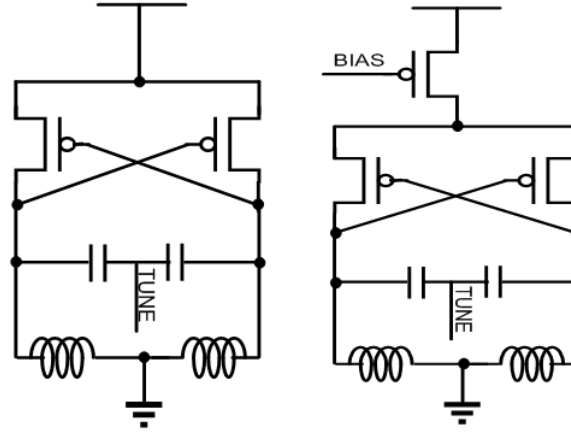


Figure 2.6: (a) PMOS VCO; (b) PMOS VCO with header

structure as the PMOS performance in terms of transconductance, phase noise and power is very different from the NMOS topology. The reason for these changes are the reduced mobility of holes in the PMOS devices.

Figure 2.6b shows the LC VCO based on PMOS devices with the header to control the current from the supply. It performs the other functions similar to the NMOS footer such as power control and output swing control. The header is made using a PMOS which makes the device fully PMOS based. Another thing to note between PMOS and NMOS devices are that in the case of PMOS device the inductor is not directly connected to the power supply so it is less prone to the supply noise. But the ground noise could be a concern in PMOS devices. A study on the effect of supply and ground noise on LC oscillator is done in [15].

In figure 2.7, a complementary LC VCO is shown. It combines the feature of both PMOS only LC VCO and NMOS only LC VCO. One of the advantages of this device is that the voltage swing is clipped to  $V_{DD}$  by PMOS and to the ground by NMOS and hence it provides a voltage swing between ground and  $V_{DD}$ . This is important because higher voltage swing induces stress in the transistors which can lead to reliability issues. One more advantage is the fact that this is more attractive to CMOS technologies because it shows immunity against process variation due to the presence of both the devices [13]. The rise and the fall symmetry reduce the  $1/f$  noise upconversion [16]. One

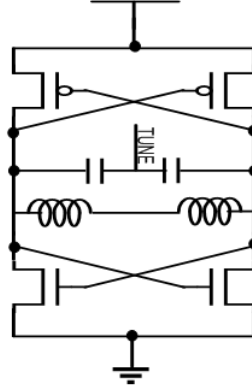


Figure 2.7: Complementary LC VCO

of the obvious disadvantages of this device is the increase in area due to the increase in the transistor counts but it is not significant as the size of the design is largely inductor dominated. Also, this structure may result in larger noise due to the existence of more noise sources.

In this work NMOS only 2.5a, PMOS only 2.6a and NMOS PMOS complementary 2.7 architectures are compared.

## 2.4 LC VCO Design Issues

There are different design parameters such as tank amplitude noise sources and header/footer noise source which has to be considered during the analysis and design of CMOS LC VCOs. These issues have been analyzed in depth in [7]. This section will give an introduction to the issues such as tank amplitude, phase noise and tuning range. An expression for tank amplitude can be obtained by assuming that the current in the differential pair instantaneously switches from one side to another. In this case the differential pair can be modeled as a current source which switches from  $I_{tail}$  to  $I_{tail}$  in parallel with the LC tank which is shown in figure 2.8 [7]. The current waveform can be assumed to be perfectly sinusoidal at high frequencies and in this case the tank amplitude can be approximated as  $V_{tank} \approx I_{tail}R_{eq}$  where  $R_{eq}$  is the equivalent resistance of the tank. This mode of operation is termed as the current limited regime [7] and in

this regime the tank amplitude is controlled by the tail current. The current limited is also termed as inductance limited regime [7] as they have the same concept of the total energy stored in the LC tank. These terms will be used interchangeably in this work.

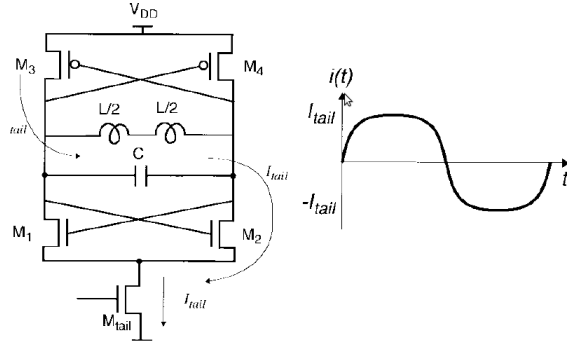


Figure 2.8: Current flow and stage switching [7]

In the case of NMOS oscillator, the tank voltage is clipped at ground and at  $V_{DD}$  in the case of PMOS only oscillators. This region is termed as voltage limited regime and is shown in figure 2.9 [7]. Hasse, et al. [13] analyses the results with constant device sizes and at the same frequency. They have used ideal inductors and capacitors for the simulation in their design. All the analysis in this work is done at the corner of current and voltage limited regime to minimize the waste of inductance in the case of the current limited regime and the waste of power in the voltage limited regime [7]. The reason for analysis at this regime is that the NCR (noise-to-carrier ratio) is the least at the boundary of current limited and voltage limited regime and is shown in figure 2.9 [7]. Also, the oscillation voltage does not get chopped at its maximum/minimum and hence it represents a good approximate sinusoidal. This prevents the sub harmonics to be present in the frequency domain.

Another important issue in the design of VCOs is the minimization of phase noise. The lower the phase noise the higher the frequency stability. Phase noise is basically a random fluctuation in the frequency of a signal and can be related to the jitter in time domain. It is expressed as the signal to noise power for a given frequency range at a given offset from the oscillating frequency and the unit is dBc/Hz. In a VCO, the phase noise can have effect from the upconversion of white and flicker noise and

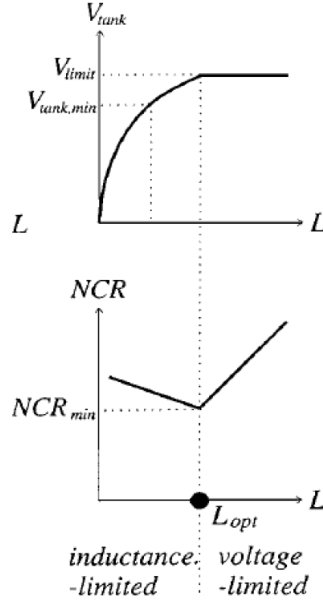


Figure 2.9:  $V_{tank}$ , NCR and operation regime [7]

the changing phase of the noise sources modulating the oscillating frequency [17]. The model for noise spectrum was given in [18] and has been used extensively in research. According to the IBM design manual used in this work, the noise model, implemented for the 32SOI FETs with BSIMSOI4.3 [19] incorporates several noise mechanisms. They are described as follows a) Flicker noise - They result from trapping and reemitting of electrons due to oxide and interface states. This noise is given by simplified Leeson's equation [20] which is given by

$$L(\Delta\omega) = \frac{KTR_{eff}[1 + A](\frac{\omega_0}{\Delta\omega})^2}{V_0^2}$$

where  $R_{eff}$  is the equivalent series resistance,  $V_0$  is the peak oscillation amplitude and  $A$  is the excess noise factor. The parameter,  $A$  is generally set to the oscillator startup safety factor. b) Thermal noise - This is due to lattice/impurity electron scattering. c) Randomness noise - Randomness of the electron injection process over the barrier leading to shot noise and is given by  $S_i = 2qIA^2/\text{Hz}$ , with  $q = 1.6 \times 10^{-19}$  C and  $I$  the dc current. An example for this type of electron injection process is the gate leakage.

d) Classical thermal noise - This includes the thermal noise of resistor elements of FET such as source resistance and drain resistance. This noise is given by  $S_i = 4kTRA^2/Hz$  where  $k$  is the Boltzmanns constant,  $T$  is the temperature, and  $R$  is the resistance. For VCO circuits the major factor for the phase noise is the low frequency device noise converted to the carrier frequency. Flicker ( $1/f$ ) noise is the major concern for the LC VCO and it shows the slope of  $-6dB/octave$  [17]. Figure 2.10 adapted from [17] shows the slope of phase noise with different noise regime.

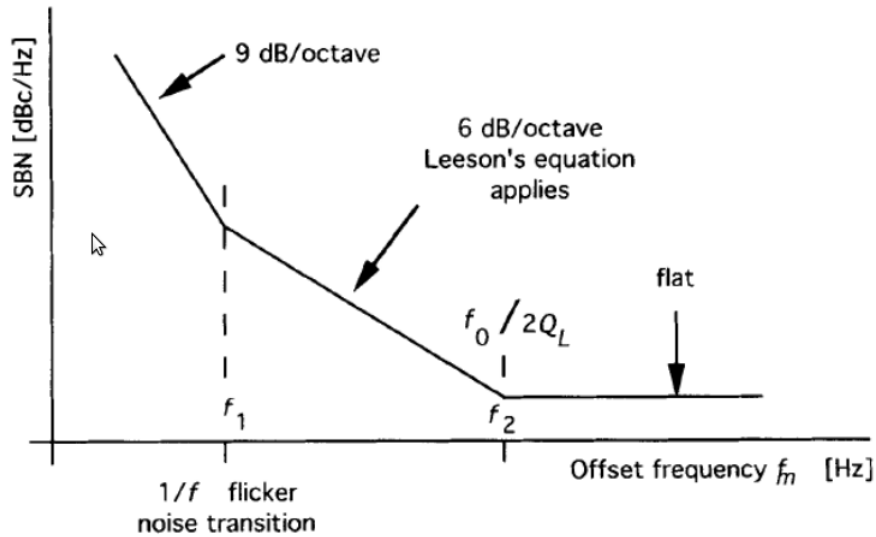


Figure 2.10: Phase noise and frequency offset [17]

The simulation results showed the VCO architectures to show a slope of almost 30dB/decade and thus the operation of the devices is in the  $1/f$  domain. Further analysis for the implemented devices is done in the results section. Flicker noise is given by the following equation (adapted from [21]):

$$\bar{V}_n^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}$$

Also, [21] states that the PMOS transistor is believed to have lower flicker noise when compared to the NMOS transistor, due to the fact that PMOS transistor carries hole in a buried channel. However, it is also mentioned in [21] that this difference in PMOS

and NMOS transistors are not consistently observed. It was seen that for this process PMOS shot noise [19] is almost two orders smaller than the NMOS. Hence if other design parameters remain same, PMOS is expected to perform better in phase noise performance.

VCO tuning range is design issue which a designer has to consider. The center frequency of a LC VCO is given by  $\frac{1}{2\pi\sqrt{LC}}$  where L is the inductance and C is the total capacitance of the tank. A varactor is used for forming the required LC tank. A varactor is basically a variable capacitor whose capacitance can be changed by changing the voltage difference between its two plates. The quality factor for inductance is directly proportional to its inductance and generally it is the inductor which decides the quality factor of the LC tank. But there are two major impacts when a designer tries to increase the inductance. First, the area of the design becomes huge and second the parasitic capacitance of the inductor limits the capacitance of the varactor and thus the range over which the capacitance can vary. As the parasitic capacitance becomes huge, the tuning capability of the varactor decreases. Table 2.2 gives the tuning range of some of the earlier works in this area.

Author	Tuning range (MHz)	Center frequency (GHz)
Craninckx [22]	250	1.8
Lam [11]	320	2.6
Razavi [10]	120	1.8
Herzel [23]	250	1.9

Table 2.2: Tuning range

In summary, this section explains the various parameters which are critical in the design of an LC VCO. Next section will cover how individual devices are chosen based on the design requirements for the LC VCOs.

## Chapter 3

# Devices for LC VCO

As the name suggests an LC VCO is composed of an oscillating tank formed by an inductor and a capacitor. It also needs a cross coupled MOS pair to provide negative resistance to make the oscillations continue. This section will discuss the devices for the LC VCO.

### 3.1 On-chip Inductors

There are different types of on-chip geometries which can be used in the VCO design such as spiral, square, hexagonal and octagonal. Spiral inductors are used in this design, so rest of the discussion will assume the use and characterization using spiral inductor. Inductance for a spiral inductor is given by the following equation:

$$L = \frac{\mu_0 K N^2 A}{l}$$

where  $L$  = inductance in henries (H),  $\mu_0$  = permeability,  $K$  = Nagaoka coefficient (value between 0 and 1),  $N$  = number of turns,  $A$  = area of cross section of coil ( $\text{m}^2$ ) and  $l$  = the length of the coil (m). The quality factor of an inductor is basically the ratio of its inductive reactance to its resistance (at a given frequency), which is also a measure of its efficiency. Another definition that is rife in designers is that the quality factor (Q) is the peak energy stored per cycle divided by the average power dissipated per cycle for a reactive element with resistive losses. The higher the Q factor of the inductor, the lesser is the losses in it and the more it resembles an ideal inductor. The



quality factor of an inductor is defined by the following equation:

$$Q = \frac{\omega L}{R}$$

where  $Q$  = quality factor,  $\omega$  = the center frequency of oscillation,  $L$  = inductance of the coil and  $R$  is the series resistance of the coil.

For VCO with 2 GHz frequency, in this design an inductance of 4.23 nH for each inductors was selected for the design. This design was chosen based on the optimization of the  $Q$  value for the design. Usually smaller inductors have the highest  $Q$  at higher frequency. Any smaller inductor would deteriorate the  $Q$  value of the design. For the generation of this inductance value an outer diameter of  $250\mu$ , metal width of  $10\mu$ , number of turns was set to 4 and the space between the turns was set to  $3\mu$ . These numbers are fixed by the design process and are designed to provide the required inductance value. The quality factor of an inductor is directly proportional to the frequency of oscillation, and the design process defines the peak  $Q$  frequency as 5.1 GHz, whereas this design is made to operate at 2 GHz. The peak  $Q$  frequency is approximated to be 9 at  $25^\circ\text{C}$  as per the design manual and thus the  $Q$  of this inductor becomes approximately 3.6. Also, the ground plane was chosen to be of M1 which makes the quality better by almost 0.5. The reason of the use of shield is to terminate the parasitic electric field from the spiral before it reaches the substrate, thus lowering substrate losses [19]. It should also be noted that for all geometries the self-resonant frequency is less for M1 groundplanes in comparison to SX inductors [19]. There are usually two types of losses which occur in an on chip inductors and they are a) skin effect loss and b) proximity effect loss. Skin effect loss is due to the fact that the resistance of the inductor increases as the square root of the frequency increase and thus the losses also increase. In a spiral inductor the enhanced magnetic field that exists in the central portions of the spiral causes nonuniform current flow in the turns and this non-uniform current flow is typically called proximity effect and tends to cause effective spiral resistance to rise faster than can be attributed to skin effect. Figure 3.1 shows the inductor used in this design and table 3.1 shows the different inductor structures, inductance and the frequency for the highest  $Q$  values. The list is not comprehensive but a trend can be noted and used to maximize the  $Q$  using the behavior shown in table 3.1.

As stated an inductor with  $N = 4$  and space between the turns of  $3\mu\text{m}$  was chosen. Increasing  $N$  would increase the inductance and make the frequency for maximum  $Q$  closer to our desired 2 GHz range but it will also increase the resistance which can deteriorate the  $Q_{max}$  value and in turn  $Q$  at 2 GHz. An analysis of the  $Q_{max}$  and inductance was done in [24] and is shown in figure 3.2 [24]. [24] shows that as the inductance increases the maximum quality factor also decreases, thus proves that improving the number of turns after a particular point will lead to reduction in the quality factor of the inductor. This analysis is a rough estimate and based on the design manual data which was limited in terms of sweeping of parameter. As we increase the number of turns, initially  $Q_{max}$  increases but beyond a point it decreases and thus making the overall quality of the inductor highest at a particular number of turns.

N	Space( $\mu\text{m}$ )	Frequency for $Q_{max}$ (GHz)
2	3	10.91
3	3	6.84
4	3	5.1
5	3	4.2
6	3	3.7
2	5	11.26
3	5	7.23
4	5	5.51
5	5	4.66
6	5	4.22

Table 3.1: Inductor parameters and quality

## 3.2 Transistor Sizing

Transistor sizing is required to provide the sufficient negative resistance to keep the oscillation continue. Also, sizing of the transistors is required to make the VCO at the boundary of current and voltage limited regime. To get to the boundary of the current limited and voltage limited regime, DFT simulations were done for the signal and peak magnitude was noted. When the peak was at its maximum the VCO is operating at the desired regime. The reason for this being that at this point the signal represents almost

Parameter	Value
Outer diameter ( $\mu\text{m}$ )	250
Metal width ( $\mu\text{m}$ )	10
Number of turns	4
Interwinding space, S (m)	3
Inductance (nH)	4.23
Peak Q frequency (GHz)	5.1

Table 3.2: Final parameter for the integrated inductor

the perfect sinusoid and the magnitude of the signal at the central frequency is at the maximum. Any larger size of the transistors will make the other harmonics amplified and thus increasing the magnitude of the sidebands in the DFT analysis.

The first step to decide the transistor size is to compensate for loss in the tank. The tank resistance can be calculated using the formula

$$R_{tank} = Q\omega L$$

Therefore in order to ensure oscillations, and to compensate for the tank losses, negative resistance should be greater than the tank resistance in magnitude. The negative resistance for the NMOS only architecture in figure 2.5 is given by  $(\frac{-2}{g_m})$ , and according to the design manual the NMOS transconductance is approximately  $1\text{S}/\mu\text{m}$ . Thus in order to start oscillations  $R_{tank}$  should be greater than magnitude of  $(\frac{-2}{g_m})$ . This determines the minimum width of the cross coupled transistors which is required to continue the oscillation. The motive of this design is to make the VCO architectures oscillate at the boundary of current limited and voltage limited regime. An analysis to decide the transistor sizing will be shown for the architecture in figure 2.5 and the rest of the architecture will be sized based on the same principle. The method of DFT analysis is chosen and for that the transistor sizes for the cross coupled MOSFETs are increased so that it shows a maximum at a particular size. The magnitude of the signal is largest at its central oscillating frequency in this regime. This trend is shown in the following table 3.3 and the DFT analysis is shown in figure 3.3. We can clearly see that the maximum magnitude of 1.49 is at a frequency of 2 GHz and the sideband magnitude is at 0.06V.

Width $\mu\text{m}$	Magnitude (V) (at 2GHz)	Magnitude of next sideband (V)
1.8	0.338	0.325
2.2	0.9	0.1335
2.6	1.08	0.072
3	1.16	0.123
3.4	1.22	0.161
4	1.29	0.173
5	1.4	0.89
6	1.49	0.67
7	1.49	0.69
8	1.42	0.79

Table 3.3: Transistor width and signal magnitude

Thus a size of  $6\mu$  for the NMOS pair is selected for the architecture 2.5. Similar analysis is done for rest of the architecture and their sizes are determined which are listed in table 3.4.

Architecture	Transistor Size ( $\mu\text{m}$ )
NMOS only (2.5(a))	6
PMOS only (2.6(a))	5
Complementary (2.7)	30(pmos)/20(nmos)

Table 3.4: Architecture and transistor sizing

### 3.3 Varactor

Varactors are an important component of a LC VCO as this is the device which is used to tune the frequency of a VCO. MOS varactors are used for this design process. It has similar properties of a parallel plate capacitor with the gate of the device forming one plate and drain, source and bulk forming the other. A non-linear relation is shown between the capacitance and the gate-bulk voltage and is very similar to the figure 4.2.

Once the inductor value is decided the capacitance can be calculated using the

formula  $\frac{1}{2\pi\sqrt{LC}}$ . For the inductance of 4.93nH and the center frequency of 2 GHz, the capacitance comes out to be approximately  $0.32 \times 10^{-12}$ F for a single varactor. An important observation was done during the simulations that a large component of this capacitance comes from the parasitic capacitance of inductors and MOSFETS. This way the designers tend to have lesser control over the tuning range and should be given a thought while deciding the sizes of the devices. The tuning range for this device will be discussed further in the results section. A study of previous work and tuning range is shown in table 2.1. For this design UGNCAP [19] was selected for the varactor which is basically a NMOS varactor with input parameter specification for width, length and total number of gates. This device is a tunable capacitor with an n-doped well and with source and drain shorted together. The gate to diffusion voltage can be varied between -0.9V to 0.9V to achieve the required variable capacitance. The model allows this variation to be between -0.5V to 0.9V. In this work the tuning voltage is varied from 0V to 0.9V to establish the tuning range for the LC VCOs and is further discussed in the result section. Layout with length as  $0.230\mu$ , width as  $10\mu$ , number of gates as 10 is shown in figure 3.4.

The parasitic capacitance varies with the architecture used, as the bias point for the varactor is largely dependent on the voltage swing of the node and thus the capacitance. Most of this parasitic capacitance comes from the inductor itself. This simulation was done with supply voltage as 0.9V, frequency of simulation as 2 GHz, at 25°C and the DC tuning voltage of 0 was selected for this simulation. For this architecture the varactor dimensions are length =  $0.230\mu$ , width =  $9\mu$ , number of fingers = 10 and the number of repetitions = 1. Similar simulations were done for all the architectures and table 3.5 enumerates the varactor parameters used for generating the required frequency.

Architecture	Varactor width ( $\mu\text{m}$ )
NMOS only (2.5(a))	9
PMOS only (2.6(a))	22
Complementary (2.7)	9

Table 3.5: Architecture and varactor size

The reason for the larger size of the varactor in the case of PMOS only architecture

is that the voltage swing at one of the inputs of the varactor is biased very close to the ground and thus it has negligible voltage difference between its two terminals (since the tuning voltage is set to ground). And for this reason the varactor size in PMOS only has to be increased in order to provide the required capacitance. Whereas in the case of NMOS only VCO, the node voltage is biased close to the supply voltage and which creates the sufficient voltage difference across the varactor terminal and thus it needs lower size. It is interesting to note that the complementary structure which is biased at almost half the supply voltage also has the varactor size same as the NMOS only architecture. The fact that the capacitance of the varactor starts to saturate as soon as the voltage difference becomes greater than 0.5V [19], ensures that they both will require the same sizing. An important characteristic regarding the phase noise was seen while using UGNCAP which showed that when the varactor size is doubled the phase noise gets worse by 6dB ( $\approx 20\log(2)$ ) which is due to the reduction in the quality of the LC tank.

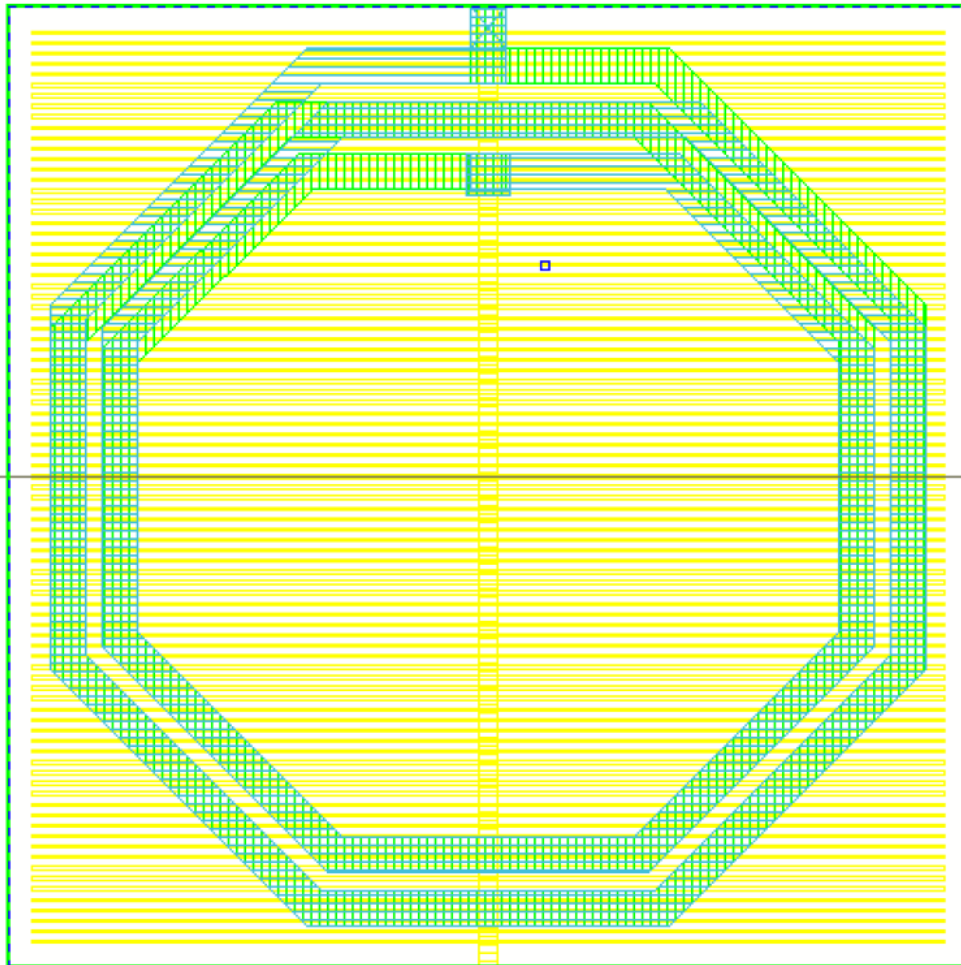


Figure 3.1: Inductor used in the design

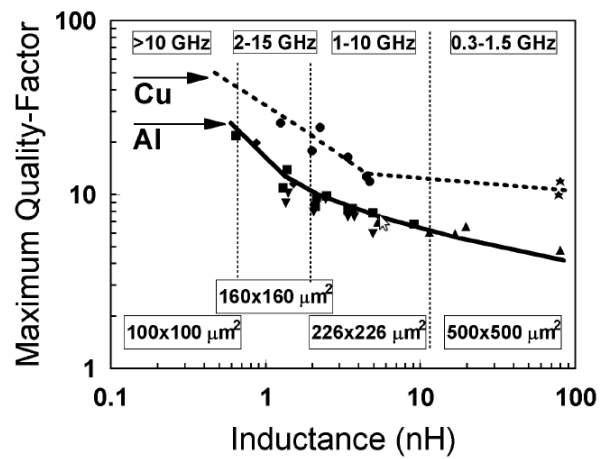
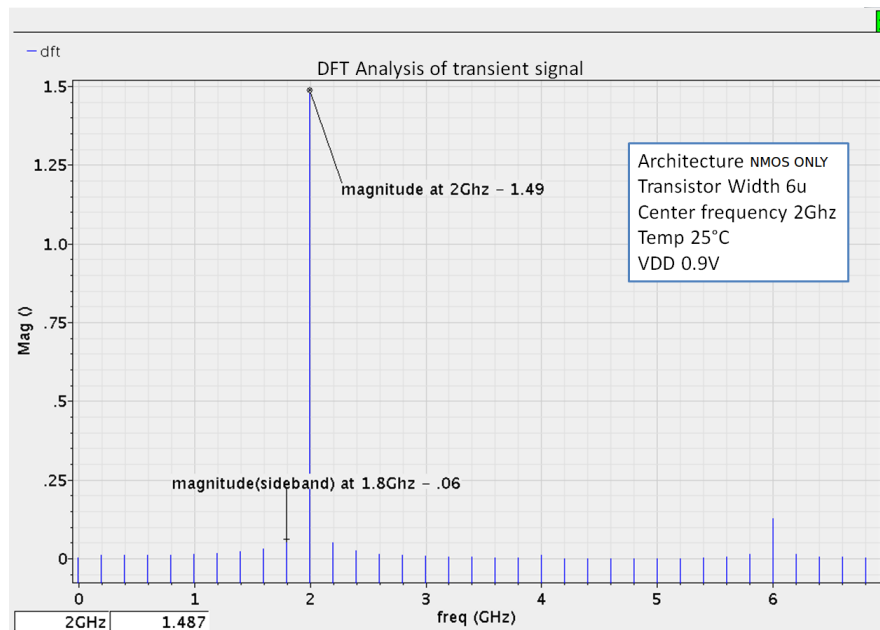
Figure 3.2:  $Q_{max}$  and inductance [24]

Figure 3.3: DFT analysis for the architecture 2.5a



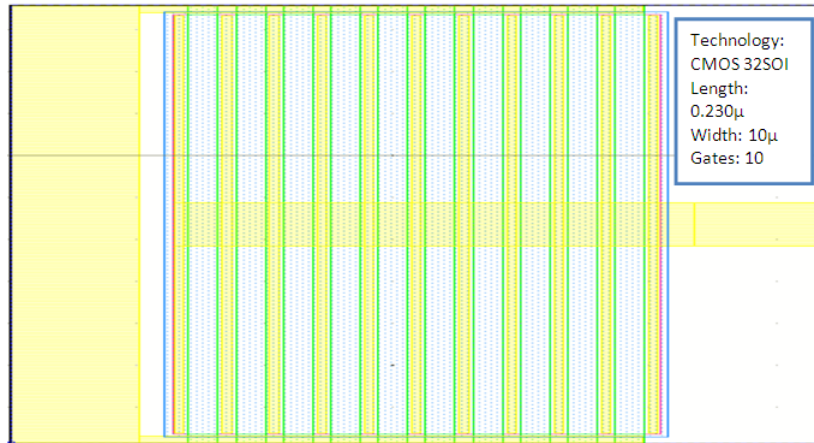


Figure 3.4: Varactor

## Chapter 4

# Simulation Results on 32nm SOI Process

Once the device dimensions have been established, the three architectures were tested for the tuning range, power, phase noise. The area was limited by the each inductor size of  $250\mu\text{m} \times 250\mu\text{m}$ , hence there were not significant difference in their areas.

### 4.1 Tuning Range

The tuning voltage was varied between 0V and 0.9V and the tuning range for the LC VCO was seen. The tuning range of different architectures is noted in table 4.1 and is shown graphically in figure 4.1.

Architecture	Tuning range (Mhz)
NMOS only (2.5(a))	350
PMOS only (2.6(a))	709
Complementary (2.7)	836

Table 4.1: LC VCO tuning range

As noted from figure 4.1, NMOS based VCO has the worst frequency tuning and the complementary NMOS PMOS VCO shows the best frequency tuning which is almost comparable to the PMOS voltage swing. The reason for this behavior is due to the

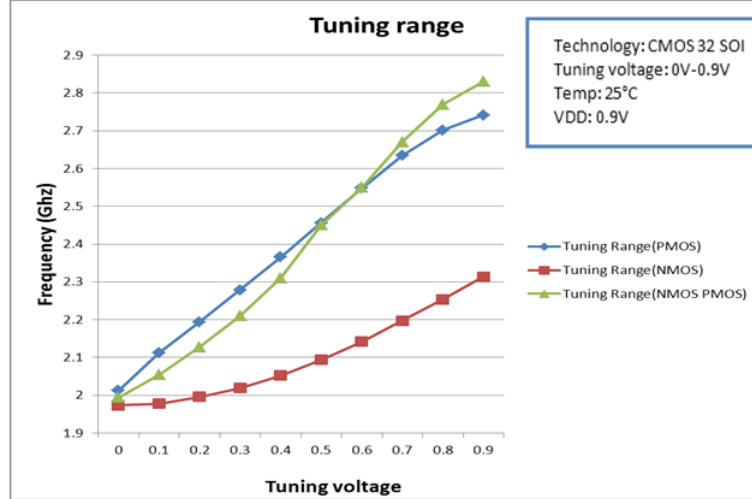


Figure 4.1: LC VCO tuning range

different bias point of the oscillating node in different VCOs. NMOS VCO is biased at approximately 0.9V and thus it gets a voltage difference across the varactor between 0V and 0.9V. Based on the similar analysis the approximate region of operation for the varactor is shown in the figure 4.2 [19]. The values of the capacitance are normalized and the purpose of this figure is just to show the trend and the region of operation of varactor in different architectures.

It should be noted that the varactor shown in 4.2 has a different size than that used in the design and the purpose of the figure is to show the region of operation as obtained from the varactor behavior in the design manual. It can be seen that the NMOS only VCO sweeps through the least part of the curve and hence the lower tuning range.

## 4.2 Power

Power analysis for the VCO was calculated based on the following formula:

$$\text{Power} = V_{\text{supply}} \times I_{\text{supply}}$$

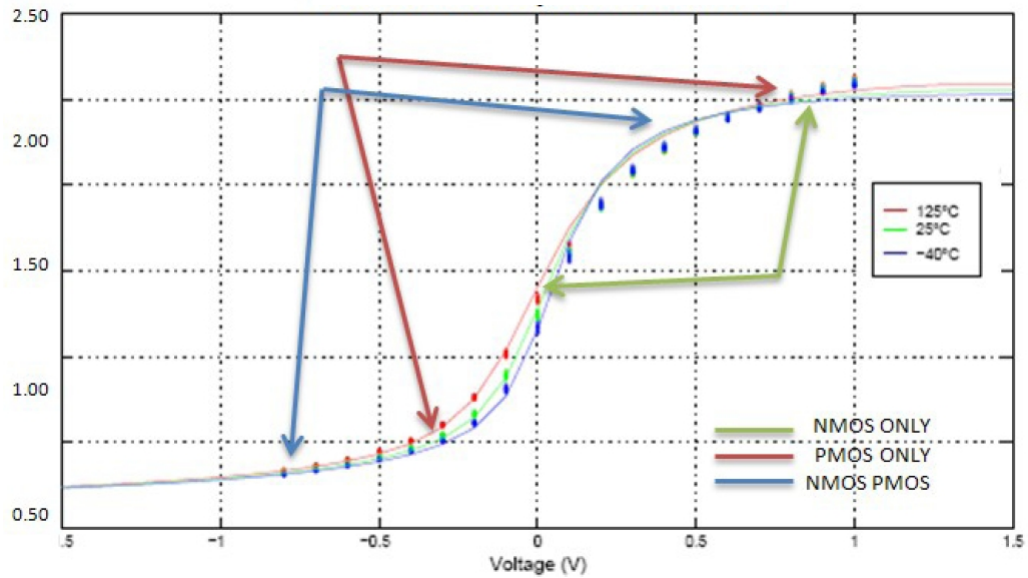


Figure 4.2: UGNCAP normalized C-V curve with region of operation

The result obtained is shown in table 4.2. A comparison of LC VCO power numbers from other literatures is shown in table 2.1.

Architecture	Power (mW)
NMOS only (2.5(a))	4.23
PMOS only (2.6(a))	1.63
Complementary (2.7)	3.53

Table 4.2: VCO power numbers

### 4.3 Voltage Swing

The voltage swing of the LC VCO is another important parameter which a designer has to consider. Since the voltage swing, if larger than the nominal supply voltage can lead to reliability issues, it must be considered during the design. The devices in this design

is operated at the boundary of voltage and current limited regime. Hence, the voltage swing of NMOS only and PMOS only devices are larger than the normal voltage swing which is between supply voltage and ground. In the case of NMOS only devices the voltage swing is clipped at ground and in the case of PMOS only devices it gets clipped at the supply voltage. The complementary structure swings between ground and supply voltage. A comparison of voltage swing among different architectures is shown in table 4.3.

Architecture	Voltage swing range(V)
NMOS only (2.5(a))	0-1.7
PMOS only (2.6(a))	-1.5-0.76
Complementary (2.7)	0-.91

Table 4.3: VCO voltage swing

## 4.4 Phase Noise

Phase noise is an important parameter for the performance of LC VCOs. A phase noise comparison of different literature is done in table 2.1. The fundamentals of phase noise are also discussed in section 2.4. All the architectures considered are made to operate at the boundary of voltage and current limited regime and the phase noise is compared in the best and the worst case. It was seen that the slope of the phase noise simulation is at 30dBc/decade, and hence it was concluded that the main source of noise in the VCOs is the flicker noise as shown in figure 2.10. Figure 4.3 shows the slope of the phase noise from architecture shown in figure 2.6a. Similar study was done for the architectures shown in figure 2.5a and 2.7 and similar slope was found. Best case phase noise is when the temperature is minimum (0°C in this design) and the oscillating frequency is the minimum ( $\approx 2$  GHz) and the result is plotted in figure 4.4 and tabulated in table 4.4. Worst case phase noise is when the temperature is maximum (125°C in this design) and the oscillating frequency is the maximum for that architecture which is approximately 2.7 GHz for PMOS only design, 2.3 GHz for NMOS only design and 2.8 GHz for NMOS PMOS design. The minimum frequency was set at 2 GHz. Worst case phase noise

is plotted in figure 4.5 and tabulated in table 4.4. Best and worst case situation was decided based on the Leeson's equation described in section 2.4.

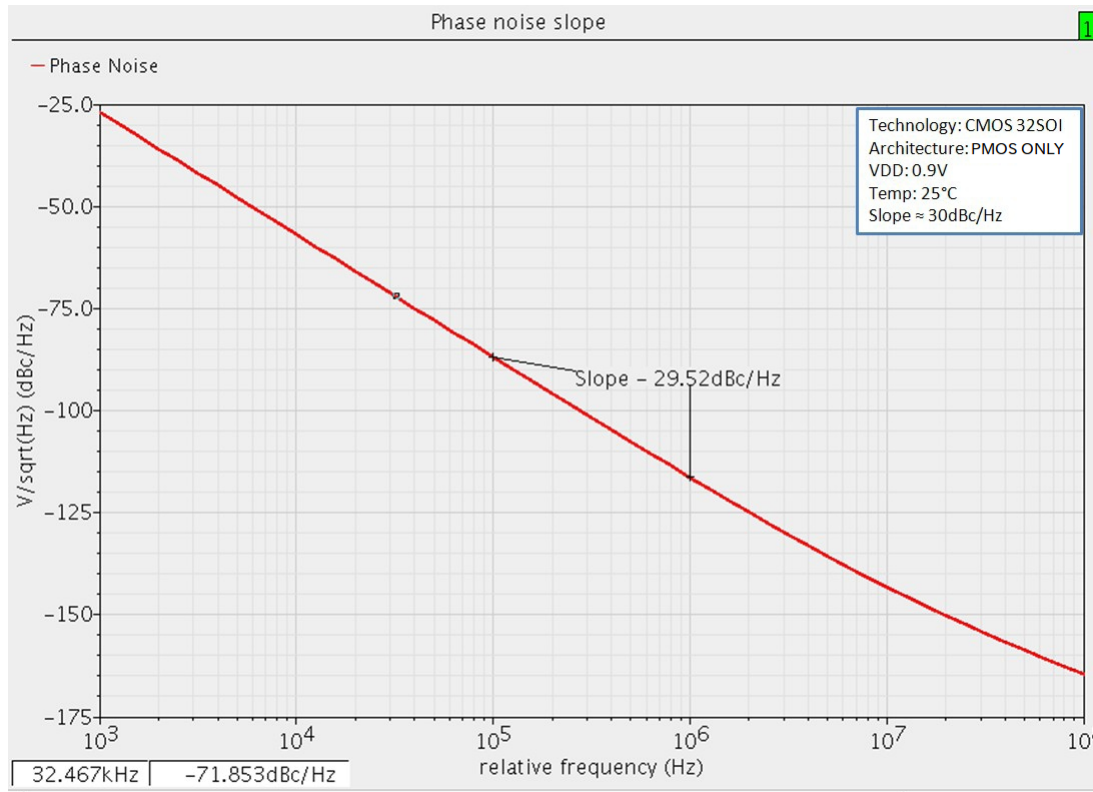


Figure 4.3: Phase noise slope

As shown in the simulation the PMOS LC VCO performance is better than the other two architectures. The reason for this effect is due to the inherent lesser flicker noise in PMOS [13]. NMOS PMOS VCO performance is slightly lesser than PMOS only VCO and this also can be attributed to larger flicker noise in NMOS devices. In the worst case, the complementary VCO performance is degraded and it becomes the worst. This effect is due to the increased noise in the  $1/f^3$  region and the AM/PM conversion of the switching noise of the cross coupled NMOS PMOS pair [13]. This effect of the NMOS PMOS VCO is shown in figure 4.6 and it can be seen that the slope of the phase noise becomes -22dB/dec at around 1MHz from the carrier frequency. The final comparison

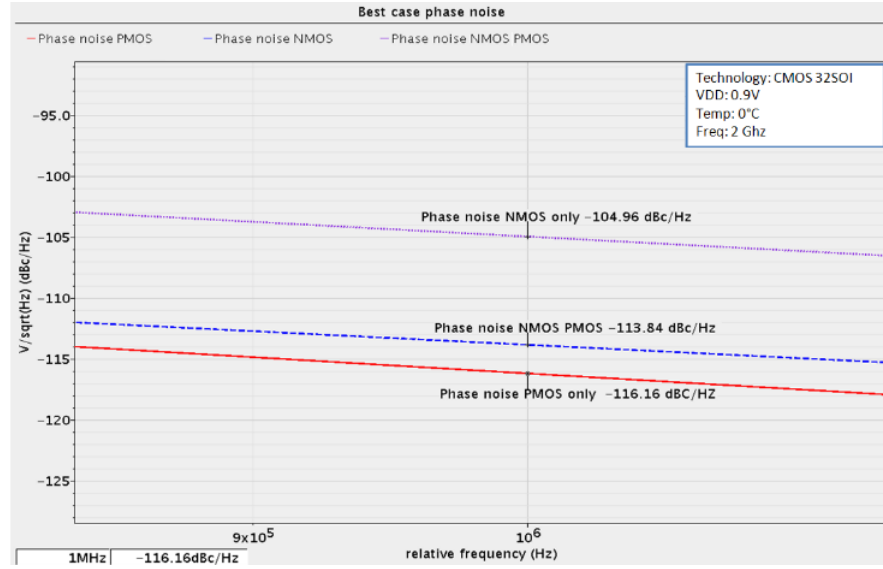


Figure 4.4: Best case phase noise

chart is given in the figure 4.7.

Architecture	Best case phase noise (dBc/HZ)	Worst case phase noise (dBc/HZ)
NMOS only (2.5(a))	-104.96	-94.04
PMOS only (2.6(a))	-116.16	-101.71
Complementary (2.7)	-113.84	-90.16

Table 4.4: Phase noise comparison

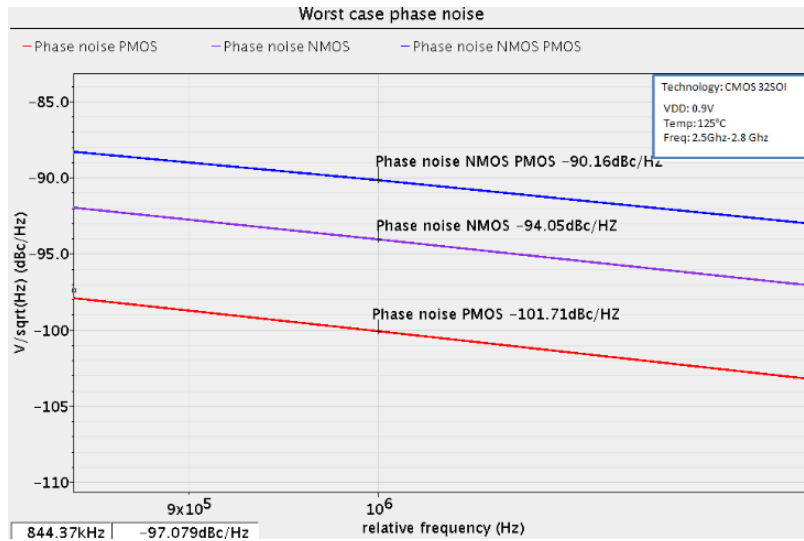


Figure 4.5: Worst case phase noise

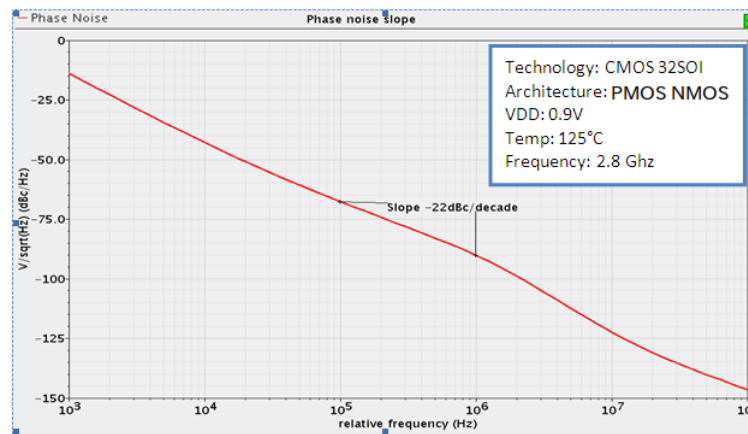


Figure 4.6: Phase noise slope



Architecture	Phase noise Best (dBc/Hz)	Phase noise Worst (dBc/Hz)	Power (mW)	Tuning Range (MHz)
NMOS only	-104.96	-94.04	4.23	350
PMOS only	-116.16	-101.71	1.63	709
Complementary	-113.84	-90.16	3.53	836

Figure 4.7: Results comparison

## Chapter 5

# Conclusion and Discussion

In this thesis, a comparison of different LC VCO architectures is done in CMOS 32nm SOI process. This comparison was done at the boundary of current and voltage limited regime and the performance parameters such as tuning range, phase noise performance, area and power dissipation have been compared. Kit inductors and varactors were used in this design. Another important observation was that the area of the LC VCOs at lower frequency is constrained by the inductor size. As the center frequency of oscillation increases, the inductance requirement decreases. This will allow designers to use smaller inductors and thus the area overhead will decrease.

Based on the comparison data, the PMOS only VCO architecture discussed in figure 2.6a proves to be the best performer with a very good tuning range, low power dissipation and good phase noise performance in the best and the worst cases. Hence it can be concluded that by suitable optimization of PMOS only VCO will perform the best in the given constraints.

As a future work, it will be a good to see the performance based on the custom inductor and their analysis based on tools such as ASITIC [25]. Using ASITIC [25] the custom inductors can be optimized based on the design frequency and area constraints and which may ultimately result in smaller and better inductors.

As we are going towards multi-GHz domain [26], a comparison of these LC VCOs at different higher frequencies in the range of 10 GHz - 20 GHz can also be a good candidate for the future work.

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